Agilex™ 3 FPGAs and SoCs Device Data Sheet

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848370
2025.10.27

Contents

848370 | 2025.10.27

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Agilex™ 3 FPGAs and SoCs Device Data Sheet

This data sheet describes the electrical characteristics, switching characteristics, configuration specifications, and timing.

Until the data sheet status for a device reaches Final, the specifications are subject to change at any time and at Altera's discretion.

Table 1. Data Sheet Status for Agilex™ 3 FPGAs and SoCs

Devices	Specification	Package	Status
A3C 100/135	W,Y,Z	M16A	Final
A3C 100/135	Z	B18A	Final
A3C 100/135	Y	B18A	Preliminary
A3C 100/135	W,Y,Z	B23C	Preliminary
A3C 025/050/065	Y,Z	B18A	Preliminary
A3C 025/050/065	Y,Z	B18B	Preliminary

The following descriptors designate the status level currently applicable to the relevant variant:

- Advance: These are target specifications based on simulation.
- Preliminary: These specifications are based on simulation, early validation, and/or early characterization data.
- Final: These are production specifications based on silicon validation and/or characterization.

Table 2. Device Grades, Core Speed Grades, and Power Options Supported

For specification status, see the *Data Sheet Status* table

Series	Temperature Grade	Speed Grade and Power Option Supported
C	Extended / Industrial	–6S (fastest)
		–7S

The suffix after the speed grade denotes the power options offered.

- S—standard power (fixed voltage)

Electrical Characteristics

Operating Conditions

The devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 3. Agilex™ 3 FPGAs Absolute Maximum Ratings

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CC}	Core voltage supply	Fixed voltage: –6S	–0.5	1.043	V
		Fixed voltage: –7S	–0.5	1.004	V
V_{CCP}	Periphery supply voltage for the I/O banks	Fixed voltage: –6S	–0.5	1.043	V

continued...

Symbol	Description	Condition	Minimum	Maximum	Unit
		Fixed voltage: –7S	–0.5	1.004	V
V_{CCH_SDM}	SDM block transceiver supply voltage sense	Without Transceiver: –6S	–0.5	1.043	V
		Without Transceiver: –7S	–0.5	1.004	V
		With Transceiver	–0.5	1.332	V
V_{CCPT}	Power supply for I/O, DTS, SDM, and system PLL	—	–0.5	2.08	V
$V_{CCRCORE}$	Power supply for programmable power technology	—	–0.5	1.64	V
$V_{CCIO\_PIO\_SDM}$	SDM block I/O supply voltage sense of bank 3A	1.2 V	–0.5	1.6	V
$V_{CC\_IO\_SDM}$	I/O digital supply voltage sense in SDM block	Fixed voltage: –6S	–0.5	1.043	V
		Fixed voltage: –7S	–0.5	1.004	V
V_{CCIO_SDM}	SDM block configuration pins power supply	—	–0.5	2.08	V
$V_{CCL\_ADC\_SDM}$	Periphery digital supply voltage sense to ADC, senses HPS digital supply on HPS devices, core supply on non-HPS devices	Fixed voltage: –6S	–0.5	1.043	V
		Fixed voltage: –7S	–0.5	1.004	V
V_{CCL_SDM}	SDM digital power supply	Fixed voltage: –6S	–0.5	1.043	V
		Fixed voltage: –7S	–0.5	1.004	V
$V_{CC\_HSSI\_L1}$	Transceiver, system PLL, and hard IP digital power supply	Fixed voltage: –6S	–0.5	1.043	V
		Fixed voltage: –7S	–0.5	1.004	V
$V_{CCPLLDIG\_SDM}$	SDM block PLL digital power supply	Fixed voltage: –6S	–0.5	1.043	V
		Fixed voltage: –7S	–0.5	1.004	V
V_{CCPLL_SDM}	SDM block PLL analog power supply	—	–0.5	2.08	V

continued...

Symbol	Description	Condition	Minimum	Maximum	Unit
$V_{CCFUSEWR\_SDM}$	Fuse block writing power supply	—	–0.5	2.08	V
V_{CCADC}	ADC voltage sensor power supply	—	–0.5	2.08	V
V_{CCL_HPS}	HPS DSU voltage and periphery circuitry power supply	Fixed voltage: –6S	–0.5	1.043	V
		Fixed voltage: –7S	–0.5	1.004	V
$V_{CCL\_HPS\_CORE0\_CORE1}$	HPS A55 cores power rail	Fixed voltage: –6S	–0.5	1.043	V
		Fixed voltage: –7S	–0.5	1.004	V
$V_{CCPLLDIG1\_HPS}$	HPS PLL1 digital power supply	Fixed voltage: –6S	–0.5	1.043	V
		Fixed voltage: –7S	–0.5	1.004	V
$V_{CCPLLDIG2\_HPS}$	HPS PLL2 digital power supply	Fixed voltage: –6S	–0.5	1.043	V
		Fixed voltage: –7S	–0.5	1.004	V
V_{CCPLL1_HPS}	HPS PLL1 analog power supply	—	–0.5	2.08	V
V_{CCPLL2_HPS}	HPS PLL2 analog power supply	—	–0.5	2.08	V
V_{CCIO_HPS}	HPS I/O buffers power supply	—	–0.5	2.08	V
V_{CCEHT_GTSL1A}	Transceiver PMA, TX PLL, transceiver reference clock, and global reference clock high-voltage analog power supply	—	–0.5	2.08	V
V_{CCERT_GTSL1A}	Transceiver PMA, transceiver reference clock, and global reference clock low-voltage analog power supply	—	–0.5	1.34	V
V_{CCIO_PIO}	HSIO bank power supply	V_{CCIO_PIO} = 1.0 V	–0.5	1.365	V
		V_{CCIO_PIO} = 1.05 V	–0.5	1.43	V

continued...

Symbol	Description	Condition	Minimum	Maximum	Unit
		V_{CCIO_PIO} = 1.1 V	–0.5	1.5	V
		V_{CCIO_PIO} = 1.2 V	–0.5	1.64	V
		V_{CCIO_PIO} = 1.3 V	–0.5	1.74	V
V_{CCIO_HVIO}	HVIO bank power supply	V_{CCIO_HVIO} = 3.3 V	–0.5	3.74	V
		V_{CCIO_HVIO} = 2.5 V	–0.5	2.83	V
		V_{CCIO_HVIO} = 1.8 V	–0.5	2.04	V
V_{CCPT_HVIO}	Supply voltage for 1.8 V I/O	—	–0.5	2.04	V
V_I	DC input voltage	V_{CCIO_PIO} = 1.0 V (1) (2)	–0.3	$V_{CCIO\_PIO(MAX)}$ + 0.25	V
		V_{CCIO_PIO} = 1.05 V (1) (2)	–0.3	$V_{CCIO\_PIO(MAX)}$ + 0.25	V
		V_{CCIO_PIO} = 1.1 V (1) (2)	–0.3	$V_{CCIO\_PIO(MAX)}$ + 0.25	V
		V_{CCIO_PIO} = 1.2 V (1) (2)	–0.3	$V_{CCIO\_PIO(MAX)}$ + 0.25	V
		V_{CCIO_PIO} = 1.3 V (1) (2)	–0.3	$V_{CCIO\_PIO(MAX)}$ + 0.25	V
		V_{CCIO_SDM} = 1.8 V	–0.3	$V_{CCIO\_SDM(MAX)}$ + 0.3	V
		V_{CCIO_HPS} = 1.8 V	–0.3	$V_{CCIO\_HPS(MAX)}$ + 0.3	V
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V	–0.3	$V_{CCIO\_HVIO(MAX)}$ + 0.3	V
I_{OUT} (3) (4)	DC output current per pin	V_{CCIO_PIO} = 1.0 V, 1.05 V, 1.1 V, 1.2 V, 1.3 V (5) (6)	–7.5	7.5	mA

continued...

(1) Applies to LVCMOS I/O standards only. For true differential input, refer to the $V_{ICM(min)}$, $V_{ICM(max)}$, and $V_{ID(max)}$ specifications.

(2) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the $V_{I(DC)}$ for the LVCMOS input can go up to $V_{CCIO\_PIO(MAX)}$ + 0.3 V.

(3) Total current per I/O bank must not exceed 100 mA.

(4) Applies to all I/O standards and settings supported by I/O banks, including single-ended and differential I/Os.

Symbol	Description	Condition	Minimum	Maximum	Unit
		V_{CCIO_SDM}, V_{CCIO_HPS} = 1.8 V (7)	–20	20	mA
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V Current Strength Setting = 12 mA(8) (9)	–8	8	mA
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V Current Strength Setting = 9 mA(8) (9)	–6	6	mA
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V Current Strength Setting = 6 mA(8) (9)	–4	4	mA
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V Current Strength Setting = 3 mA(8) (9)	–2	2	mA
T_J (10)	Absolute junction temperature	—	–40	125	°C
T_{STG}	Storage temperature	—	–55	150	°C

(5) The maximum current allowed through any HSIO pin during power-up/power-down conditions is 10 mA. Pin voltage during these conditions should not exceed 1.2 V or the V_{CCIO_PIO} supply rail of the bank where the I/O pin resides in, whichever is the lower voltage. While this device is not turned on, the I/O pin should be tri-stated or not driven with any external voltages.

(6) The DC output current per pin may exceed 7.5 mA with a duration limit. For more details, refer to the related information.

(7) The maximum current allowed through any HPS/SDM pin when the device is not turned on or during power-up/power-down conditions is 10 mA. Pin voltage during these conditions should not exceed V_{CCIO_HPS} or V_{CCIO_SDM} supply rail of the bank where the I/O pin resides in.

(8) The maximum current allowed through any HVIO pin when the device is not turned on or during power-up/power-down conditions is 10 mA. Pin voltage during these conditions should not exceed V_{CCIO_HVIO} supply rail of the bank where the I/O pin resides in.

(9) The DC output current per pin may exceed specified values with a duration limit. For more details, refer to General Purpose I/O User Guide.

(10) When using the device at T_J = 100°C, the device can operate under the recommended operating conditions over a minimum device lifetime of 11.4 years.

Related Information

- Recommended Operating Conditions on page 14
- I/O Standard Specifications on page 29
- General-Purpose I/O User Guide: Agilex 3 FPGAs and SoCs

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, the toggling input data or clock signals may overshoot to the voltage listed in the following tables and undershoot to the following limits for input currents less than 100 mA and periods shorter than 20 ns.

- Undershoot limit of –1.1 V when using V_{CCIO_HPS} or V_{CCIO_SDM} of 1.8 V.
- Undershoot limit of –0.3 V when using V_{CCIO_PIO} of 1.3 V, 1.2 V, 1.1 V, 1.05 V, and 1.0 V.

No overshooting beyond 1.65 V and undershooting below 0.273 V is allowed when using True Differential Signaling I/O standard at V_{CCIO_PIO} = 1.3 V.

No overshooting beyond 1.177 V and undershooting below 0.573 V is allowed when using True Differential Signaling I/O standard at V_{CCIO_PIO} = 1.2 V, 1.1 V, and 1.05 V.

The maximum allowed overshoot duration is specified as a percentage of high time (calculated as ([delta T]/T) × 100) over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

Table 4. Maximum Allowed Overshoot During Transitions for 1.0 V I/O in HSIO Bank

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Overshoot Duration as % at T_J = 100°C	Unit
V_i (AC)	AC input voltage	V_{CCIO_PIO} + 0.25	100	%
		V_{CCIO_PIO} + 0.30(11)	30	%
		V_{CCIO_PIO} + 0.35	4	%
		> V_{CCIO_PIO} + 0.40	No overshoot allowed	%

Table 5. Maximum Allowed Overshoot During Transitions for 1.05 V I/O in HSIO Bank

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Overshoot Duration as % at T_J = 100°C	Unit
V_i (AC)	AC input voltage	V_{CCIO_PIO} + 0.25	100	%
		V_{CCIO_PIO} + 0.30(12)	30	%
		V_{CCIO_PIO} + 0.35	4	%
		> V_{CCIO_PIO} + 0.40	No overshoot allowed	%

(11) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the V_i (AC) for the LVCMOS input can go up to V_{CCIO_PIO} + 0.3 V at an overshoot duration of 100%.

(12) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the V_i (AC) for the LVCMOS input can go up to V_{CCIO_PIO} + 0.3 V at an overshoot duration of 100%.

Table 6. Maximum Allowed Overshoot During Transitions for 1.1 V I/O in HSIO Bank

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Overshoot Duration as % at T_J = 100°C	Unit
V_i (AC)	AC input voltage	V_{CCIO_PIO} + 0.25	100	%
		V_{CCIO_PIO} + 0.30[13]	30	%
		V_{CCIO_PIO} + 0.35	4	%
		> V_{CCIO_PIO} + 0.40	No overshoot allowed	%

Table 7. Maximum Allowed Overshoot During Transitions for 1.2 V I/O in HSIO Bank

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Overshoot Duration as % at T_J = 100°C	Unit
V_i (AC)	AC input voltage	V_{CCIO_PIO} + 0.25	100	%
		V_{CCIO_PIO} + 0.30[14]	30	%
		V_{CCIO_PIO} + 0.35	4	%
		> V_{CCIO_PIO} + 0.40	No overshoot allowed	%

(13) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the V_i (AC) for the LVCMOS input can go up to V_{CCIO_PIO} + 0.3 V at an overshoot duration of 100%.

(14) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the V_i (AC) for the LVCMOS input can go up to V_{CCIO_PIO} + 0.3 V at an overshoot duration of 100%.

Table 8. Maximum Allowed Overshoot During Transitions for 1.3 V I/O in HSIO Bank

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Overshoot Duration as % at T_J = 100°C	Unit
V_i (AC)	AC input voltage	V_{CCIO_PIO} + 0.25	100	%
		V_{CCIO_PIO} + 0.30[15]	65	%
		V_{CCIO_PIO} + 0.35	7	%
		> V_{CCIO_PIO} + 0.40	No overshoot allowed	%

Table 9. Maximum Allowed Overshoot During Transitions for 1.8 V I/O in HPS and SDM I/O Banks

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Overshoot Duration as % at T_J = 100°C	Unit
V_i (AC)	AC input voltage	V_{CCIO_SDM} + 0.30, V_{CCIO_HPS} + 0.30	100	%
		V_{CCIO_SDM} + 0.35, V_{CCIO_HPS} + 0.35	60	%
		V_{CCIO_SDM} + 0.40, V_{CCIO_HPS} + 0.40	30	%
		V_{CCIO_SDM} + 0.45, V_{CCIO_HPS} + 0.45	20	%

continued...

(15) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the V_i (AC) for the LVCMOS input can go up to V_{CCIO_PIO} + 0.3 V at an overshoot duration of 100%.

Symbol	Description	Condition (V)	Overshoot Duration as % at T_J = 100°C	Unit
		V_{CCIO_SDM} + 0.50, V_{CCIO_HPS} + 0.50	10	%
		V_{CCIO_SDM} + 0.55, V_{CCIO_HPS} + 0.55	6	%
		> V_{CCIO_SDM} + 0.55, > V_{CCIO_HPS} + 0.55	No overshoot allowed	%

Table 10. Maximum Allowed Overshoot During Transitions for 1.8 V, 2.5 V, and 3.3 V in HVIO Bank

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

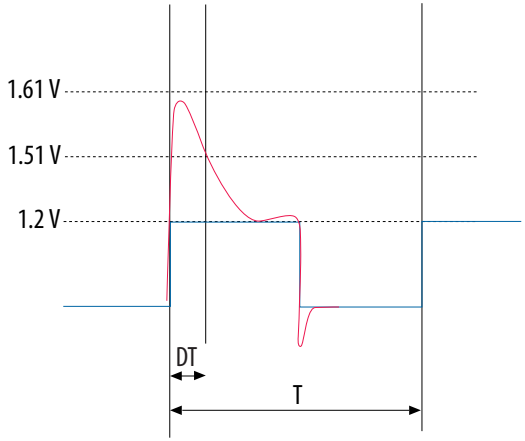
For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Overshoot Duration as % at T_J = 100°C	Unit
Vi (AC) (16)	AC input voltage	V_{CCIO_HVIO} + 0.30	100	%
		V_{CCIO_HVIO} + 0.35	42	%
		V_{CCIO_HVIO} + 0.40	18	%
		V_{CCIO_HVIO} + 0.45	9	%
		V_{CCIO_HVIO} + 0.50	4	%
		> V_{CCIO_HVIO} + 0.55	No overshoot allow	%

For example, when using 1.2 V I/O standard with 1.26 V V_{CCIO_PIO}, a signal that overshoots to 1.61 V can only be at 1.61 V for ~4% over the lifetime of the device. For an overshoot of 1.51 V, the percentage of high time for the overshoot can be as high as 100% over the lifetime of the device.

(16) This value applies to both input and output configuration.

Figure 1. Overshoot Duration Example (for 1.2 V HSIO Bank at V_{CCIO_PIO} = 1.26 V)



Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters.

Recommended Operating Conditions

Table 11. Agilex™ 3 FPGAs Recommended Operating Conditions

This table lists the steady-state voltage values expected. Power supply ramps must all be strictly monotonic, without plateaus.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Minimum[17]	Typical	Maximum[17]	Unit
V_{CC}	Core voltage supply	Fixed voltage: –6S	0.756	0.78	0.803	V
		Fixed voltage: –7S	0.7275	0.75	0.7725	V

continued...

(17) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

Symbol	Description	Condition	Minimum[17]	Typical	Maximum[17]	Unit
V_{CCP}	Periphery supply voltage for the I/O banks	Fixed voltage: –6S	0.756	0.78	0.803	V
		Fixed voltage: –7S	0.7275	0.75	0.7725	V
V_{CCH_SDM}	SDM block transceiver supply voltage sense	Without transceiver: –6S	0.756	0.78	0.803	V
		Without transceiver: –7S	0.7275	0.75	0.7725	V
		With transceiver	0.975	1	1.025	V
V_{CCPT} [18]	Power supply for I/O, DTS, SDM, and system PLL	—	1.746	1.8	1.854	V
$V_{CCRCORE}$	Power supply for programmable power technology	—	1.14	1.2	1.26	V
$V_{CCIO\_PIO\_SDM}$ [19]	SDM block I/O supply voltage sense of bank 3A	1.2 V	1.164	1.2	1.236	V
$V_{CC\_IO\_SDM}$	I/O digital supply voltage sense in SDM block	Fixed voltage: –6S	0.756	0.78	0.803	V
		Fixed voltage: –7S	0.7275	0.75	0.7725	V
V_{CCIO_SDM}	SDM block configuration pins power supply	—	1.71	1.8	1.89	V

continued...

(17) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(18) Must use a tolerance of ±3% when sharing with V_{CCIO_HVIO}. A tolerance of ±5% is only allowed when V_{CCPT} is not shared with other rails.

(19) Must be supplied at 1.2 V when using Avalon® Streaming ×16 configuration schemes. For more information, please refer to the Agilex™ 3 Device Family Pin Connection Guidelines.

Symbol	Description	Condition	Minimum[17]	Typical	Maximum[17]	Unit
$V_{CCL\_ADC\_SDM}$	Periphery digital supply voltage sense to ADC, senses HPS digital supply on HPS devices, core supply on non-HPS devices	Fixed voltage: –6S	0.756	0.78	0.803	V
		Fixed voltage: –7S	0.7275	0.75	0.7725	V
V_{CCL_SDM}	SDM digital power supply	Fixed voltage: –6S	0.756	0.78	0.803	V
		Fixed voltage: –7S	0.7275	0.75	0.7725	V
$V_{CCPLLDIG\_SDM}$	SDM block PLL digital power supply	Fixed voltage: –6S	0.756	0.78	0.803	V
		Fixed voltage: –7S	0.7275	0.75	0.7725	V
V_{CCPLL_SDM}	SDM block PLL analog power supply	—	1.71	1.8	1.89	V
$V_{CCFUSEWR\_SDM}$	Fuse block writing power supply	—	1.71	1.8	1.89	V
V_{CCADC}	ADC voltage sensor power supply	—	1.71	1.8	1.89	V
V_{CCIO_PIO}	HSIO bank power supply	1.0 V	0.95	1	1.05	V
		1.05 V[20]	1.0185	1.05	1.0815	V
		1.1 V[20]	1.067	1.1	1.133	V
		1.2 V[20]	1.164	1.2	1.236	V
		1.3 V	1.261	1.3	1.339	V

continued...

(17) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

Symbol	Description	Condition	Minimum[17]	Typical	Maximum[17]	Unit
V_{CCIO_HVIO}	HVIO bank power supply	3.3 V	3.201	3.3	3.399	V
		2.5 V	2.425	2.5	2.575	V
		1.8 V	1.746	1.8	1.854	V
V_{CCPT_HVIO}	Supply voltage for 1.8 V I/O	—	1.746	1.8	1.854	V
V_I [21]	DC input voltage	V_{CCIO_PIO} = 1.0 V[22]	–0.3000	—	V_{CCIO_PIO} + 0.25	V
		V_{CCIO_PIO} = 1.05 V[23] [22]	–0.3000	—	V_{CCIO_PIO} + 0.25	V
		V_{CCIO_PIO} = 1.1 V[23] [22]	–0.3000	—	V_{CCIO_PIO} + 0.25	V
		V_{CCIO_PIO} = 1.2 V[23] [22]	–0.3000	—	V_{CCIO_PIO} + 0.25	V
		V_{CCIO_PIO} = 1.3 V[23] [22]	–0.3000	—	V_{CCIO_PIO} + 0.25	V

continued...

(17) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(20) Each sub-bank can only support a single voltage tolerance. The V_{CCIO_PIO} tolerance can be extended to ±5% if the entire HSIO sub-bank is operating in any of the following modes:
- LVDS SERDES receiver mode with the use of 1.05 V, 1.1 V, 1.2 V True Differential Signaling input standard
- PHYLITE mode
- GPIO mode

(21) This value applies to both input and tri-stated output configuration. Pin voltage should not be externally pulled higher than the maximum value.

(22) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the $V_{I(DC)}$ for the LVCMOS input can go up to V_{CCIO_PIO} + 0.3 V.

(23) Applies to LVCMOS I/O standards only. For true differential input, refer to the $V_{ICM(min)}$, $V_{ICM(max)}$, and $V_{ID(max)}$ specifications.

Symbol	Description	Condition	Minimum[17]	Typical	Maximum[17]	Unit
		V_{CCIO_SDM} = 1.8 V	–0.3000	—	V_{CCIO_SDM} + 0.3	V
		V_{CCIO_HPS} = 1.8 V	–0.3000	—	V_{CCIO_HPS} + 0.3	V
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V	–0.3000	—	V_{CCIO_HVIO} + 0.3	V
V_O	Output voltage	V_{CCIO_PIO} = 1.0 V, 1.05 V, 1.1 V, 1.2 V, 1.3 V	0	—	V_{CCIO_PIO}	V
		V_{CCIO_SDM} = 1.8 V	0	—	V_{CCIO_SDM}	V
		V_{CCIO_HPS} = 1.8 V	0	—	V_{CCIO_HPS}	V
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V	0	—	V_{CCIO_HVIO}	V
T_J	Operating junction temperature	Extended	0	—	100[24]	°C
		Industrial	–40	—	100[24]	°C
t_{RAMP} [25] [26]	Power supply ramp time	Standard POR	200 µs	—	100 ms	—

Related Information

- I/O Standard Specifications on page 29
- Agilex 3 Device Family Pin Connection Guidelines.

(17) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(24) When using the device at T_J = 100°C, the device can operate under the recommended operating conditions over a minimum device lifetime of 11.4 years.

(25) t_{RAMP} is the ramp time of each individual power supply, not the ramp time of all combined power supplies. The ramp time applies to both the ramp-up and ramp-down of the power rails.

(26) To support AS fast mode, all power supplies to the device must be fully ramped-up within 10 ms to the recommended operating conditions.

GTS Transceiver Power Supply Operating Conditions

Table 12. Agilex 3 FPGAs GTS Transceiver Power Supply Operating Conditions

For specification status, see the *Data Sheet Status* table

Symbol	Description	Speed Grade	Typical DC Level (V)	Recommended VR Accuracy (% of Typical DC Level)	Recommended VR Ripple (% of Typical DC level)	Recommended AC Transient (% of Typical DC level)	Maximum (VR Accuracy + Ripple + AC Transient) (% of Typical DC Level)(27)	Unit
$V_{CC\_HSSI\_L1}$	Transceiver, system PLL, and hard IP digital power supply	–6S	0.78	±0.5	±2.5		±3	V
		–7S	0.75	±0.5	±2.5		±3	V
V_{CCEHT_GTSL1A} (28)	Transceiver PMA, transceiver PLL, and transceiver reference clock high voltage analog power supply	—	1.8	±0.5	±2.0		±2.5	V
V_{CCERT_GTSL1A}	Transceiver PMA and transceiver reference clock low voltage analog power supply	—	1	±0.5	±2.0		±2.5	V

(27) For scope measurement, 20 MHz bandwidth is sufficient. During measurement, put the ground pin as close to the power rail pin as possible.

(28) HF noise requires AC 30 mVpp above 1 MHz.

HPS Power Supply Operating Conditions

Table 13. HPS Power Supply Operating Conditions

This table lists the steady-state voltage and current values expected for system-on-a-chip (SoC) devices with Arm*-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus. Refer to the *Recommended Operating Conditions* table for the steady-state voltage values expected from the FPGA portion of the SoC devices.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CCL_HPS}	HPS DSU voltage and periphery circuitry power supply	Fixed voltage: –6S	(Typical) – 3%	0.78	(Typical) + 3%	V
		Fixed voltage: –7S	(Typical) – 3%	0.75	(Typical) + 3%	V
$V_{CCL\_HPS\_CORE0\_CORE1}$	HPS Cortex-A55 core 0 and core 1 power rail	Fixed voltage: –6S	(Typical) – 3%	0.78	(Typical) + 3%	V
		Fixed voltage: –7S	(Typical) – 3%	0.75	(Typical) + 3%	V
$V_{CCPLLDIG1\_HPS}$	HPS PLL1 digital power supply (can be connected to V_{CCL_HPS})	Fixed voltage: –6S	(Typical) – 3%	0.78	(Typical) + 3%	V
		Fixed voltage: –7S	(Typical) – 3%	0.75	(Typical) + 3%	V
$V_{CCPLLDIG2\_HPS}$	HPS PLL2 digital power supply (can be connected to V_{CCL_HPS})	Fixed voltage: –6S	(Typical) – 3%	0.78	(Typical) + 3%	V
		Fixed voltage: –7S	(Typical) – 3%	0.75	(Typical) + 3%	V
V_{CCPLL1_HPS}	HPS PLL1 analog power supply	1.8 V	1.71	1.8	1.89	V
V_{CCPLL2_HPS}	HPS PLL2 analog power supply	1.8 V	1.71	1.8	1.89	V
V_{CCIO_HPS}	HPS I/O buffers power supply	1.8 V	1.71	1.8	1.89	V

Related Information

- Recommended Operating Conditions on page 14
  Provides the steady-state voltage values for the FPGA portion of the device.
- HPS Clock Performance on page 69

DC Characteristics

Supply Current and Power Consumption

Altera offers two ways to estimate power for your design—the Power and Thermal Calculator (PTC) and the Quartus® Prime Power Analyzer feature.

Use the PTC before you start your design to estimate the supply current for your design. The PTC provides a magnitude estimate of the device power because these currents vary greatly with the usage of the resources.

The Quartus Prime Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yield very accurate power estimates.

HSIO DC Characteristics

HSIO I/O Pin Leakage Current

Table 14. HSIO I/O Pin Leakage Current

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIO\_PIO\ (MAX)}$	–360	360	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIO\_PIO\ (MAX)}$	–360	360	µA

HSIO OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

Table 15. HSIO OCT Calibration Accuracy Specifications

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

These specifications require RZQ reference accuracy of 240 Ω ±1%.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Calibration Accuracy	Unit
34-Ω and 40-Ω R_S (29)	Internal series termination with calibration (34-Ω and 40-Ω setting)	SSTL-12, HSTL-12, HSUL-12, and POD12 I/O standards	20	%
		POD11 and LVSTL11 I/O standards	20	%
		LVSTL105 I/O standard	20	%
45-Ω R_S	Internal series termination with calibration (45-Ω setting)	DPHY I/O standards	–20 to +25	%
50-Ω and 60-Ω R_T (29)	Internal parallel termination with calibration (50-Ω and 60-Ω setting)	SSTL-12 and HSTL-12 I/O standards	20	%
40-Ω, 50-Ω, and 60-Ω R_T (29)	Internal parallel termination with calibration (40-Ω, 50-Ω, and 60-Ω setting)	POD11 and POD12 I/O standards	20	%
		LVSTL11 and LVSTL105 I/O standards	20	%
100-Ω R_D	Internal differential termination with calibration (100-Ω setting)	DPHY I/O standards	–20 to +25	%

(29) This specification applies to both single-ended and pseudo-differential I/O buffers.

HSIO OCT Without Calibration Resistance Tolerance Specifications

Table 16. HSIO OCT Without Calibration Resistance Tolerance Specifications

This table lists the GPIO OCT without calibration resistance tolerance to PVT changes.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Calibration Accuracy	Unit
34-Ω and 40-Ω R_S	Internal series termination without calibration (34-Ω and 40-Ω setting)	1.3 V LVCMOS I/O standard	30	%
34-Ω and 40-Ω R_S (30)	Internal series termination without calibration (34-Ω and 40-Ω setting)	1.2 V LVCMOS, SSTL-12, HSTL-12, HSUL-12, and POD12 I/O standards	25	%
		1.1 V LVCMOS, POD11, and LVSTL11 I/O standards	25	%
		1.05 V LVCMOS and LVSTL105 I/O standards	25	%
34-Ω and 40-Ω R_S	Internal series termination without calibration (34-Ω and 40-Ω setting)	1.0 V LVCMOS I/O standard	30	%
50-Ω R_T (30)	Internal parallel termination without calibration (50-Ω setting)	SSTL-12 and HSTL-12 I/O standards	25	%
		POD11 and POD12 I/O standards	25	%
		LVSTL11 and LVSTL105 I/O standards	25	%
100-Ω R_D (31)	Internal differential termination (100-Ω setting)	True differential signaling I/O standard at V_{CCIO_PIO} = 1.05	40	%
		True differential signaling I/O standard at V_{CCIO_PIO} = 1.1	40	%

continued...

(30) This specification applies to both single-ended and pseudo-differential I/O buffers.

(31) This specification applies to $V_{ICM(DC)} \leq 1.3V$. For $V_{ICM(DC)} > 1.3V$, a specification range of -60% to +40% applies.

Symbol	Description	Condition (V)	Calibration Accuracy	Unit
		True differential signaling I/O standard at V_{CCIO_PIO} = 1.2	40	%
		True differential signaling I/O standard at V_{CCIO_PIO} = 1.3	40	%
100-Ω R_D	Internal differential termination (100-Ω setting)	SLVS400 I/O standard	30	%

HSIO Pin Capacitance

Table 17. HSIO Pin Capacitance

For specification status, see the *Data Sheet Status* table

Symbol	Description	Maximum	Unit
C_{IO}	Input/output capacitance of I/O pins	2.6[32]	pF

HSIO Internal Weak Pull-Up Resistor

All I/O pins in GPIO bank have an option to enable weak pull-up when using 1.0 V, 1.05 V, 1.1 V, 1.2 V, and 1.3 V LVCMOS I/O standards.

Table 18. HSIO Internal Weak Pull-Up Resistor

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Min	Typ	Max	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option.	V_{CCIO_PIO} = 1.3 ±3%	3	10	30	kΩ
		V_{CCIO_PIO} = 1.2 ±5%	3	10	30	kΩ
		V_{CCIO_PIO} = 1.1 ±5%	3	10	30	kΩ
		V_{CCIO_PIO} = 1.05 ±5%	3	10	30	kΩ
		V_{CCIO_PIO} = 1.0 ±5%	3	10	30	kΩ

(32) This value refers to die-level pin capacitance without the device package.

HVIO DC Characteristics

HVIO I/O Pin Leakage Current

Table 19. HVIO I/O Pin Leakage Current

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIO\_HVIO\ (MAX)}$	-10	10	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to V_{CCIO_HVIO} (MAX)	-10	10	µA

HVIO Pin Capacitance

Table 20. HVIO Pin Capacitance

For specification status, see the *Data Sheet Status* table

Symbol	Description	Maximum	Unit
C_{IO}	Input/output capacitance of I/O pins	4(33)	pF

HVIO Internal Weak Pull-Up and Pull-Down Resistor

Only input and bidirectional pins in HVIO bank have an option to enable weak pull-up and pull-down when using LVCMOS I/O standard.

Table 21. HVIO Internal Weak Pull-Up and Pull-Down Resistor Values

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Min	Typ	Max	Unit
20 kΩ R_{PU}, 20 kΩ R_{PD}	Value of the I/O pin pull-up and pull-down resistor during user mode if you have enabled the	V_{CCIO_HVIO} = 1.8, 2.5, 3.3 ±3%	15	20	30	kΩ

(33) This value refers to die-level pin capacitance without the device package.

Symbol	Description	Condition (V)	Min	Typ	Max	Unit
	programmable pull-up or pull-down resistor option.					

HVIO Hysteresis Specifications for Schmitt Trigger Input

Table 22. HVIO Hysteresis Specifications for Schmitt Trigger Input

This device supports built-in Schmitt trigger input that always enabled on HVIO I/O bank. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signal with slow edge rate.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Typ	Max	Unit
V_{HYS}	Hysteresis for Schmitt trigger input	V_{CCIO_HVIO} = 1.8 V	—	200	—	mV
		V_{CCIO_HVIO} = 2.5 V	—	250	—	mV
		V_{CCIO_HVIO} = 3.3 V	—	250	—	mV

HPS I/O DC Characteristics

HPS I/O Pin Leakage Current

Table 23. HPS I/O Pin Leakage Current

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIO\_HPS\ (MAX)}$	–15	15	µA
	Tri-stated I/O pin	V_O = 0 V to $V_{CCIO\_HPS\ (MAX)}$	–15	15	µA

HPS I/O Pin Capacitance

Table 24. HPS I/O Pin Capacitance

For specification status, see the *Data Sheet Status* table

Symbol	Description	Maximum	Unit
C_{IO}	Input/output capacitance of I/O pins	5[34]	pF

HPS I/O Internal Weak Pull-Up Resistor

The I/O pins in HPS bank are supported with weak pull-up and weak pull-down options.

Table 25. HPS Internal Weak Pull-Up Resistor

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Min	Typ	Max	Unit
20 kΩ R_{PU}, 20 kΩ R_{PD}	Value of the I/O pin pull-up and pull-down resistor during user mode if you have enabled the programmable pull-up or pull-down resistor option.	V_{CCIO_HPS} = 1.8 ±5%	15	20	25	kΩ
50 kΩ R_{PU}, 50 kΩ R_{PD}	Value of the I/O pin pull-up and pull-down resistor during user mode if you have enabled the programmable pull-up or pull-down resistor option.	V_{CCIO_HPS} = 1.8 ±5%	37.5	50	62.5	kΩ
80 kΩ R_{PU}, 80 kΩ R_{PD}	Value of the I/O pin pull-up and pull-down resistor during user mode if you have enabled the	V_{CCIO_HPS} = 1.8 ±5%	57	80	105	kΩ

continued...

(34) This value refers to die-level pin capacitance without the device package.

Symbol	Description	Condition (V)	Min	Typ	Max	Unit
	programmable pull-up or pull-down resistor option.					

HPS I/O Hysteresis Specifications for Schmitt Trigger Input

Table 26. HPS I/O Hysteresis Specifications for Schmitt Trigger Input

This device supports Schmitt trigger input on HPS I/O bank. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signal with slow edge rate.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Typ	Max	Unit
V_{HYS}	Hysteresis for Schmitt trigger input	V_{CCIO_HPS} = 1.8 V	180	–	–	mV

SDM I/O DC Characteristics

SDM I/O Pin Leakage Current

Table 27. SDM I/O Pin Leakage Current

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIO\_SDM\ (MAX)}$	–15	15	µA
	Tri-stated I/O pin	V_O = 0 V to $V_{CCIO\_SDM\ (MAX)}$	–15	15	µA

SDM I/O Pin Capacitance

Table 28. SDM I/O Pin Capacitance

For specification status, see the *Data Sheet Status* table

Symbol	Description	Maximum	Unit
C_{IO}	Input/output capacitance of I/O pins	5(35)	pF

SDM I/O Internal Weak Pull-Up Resistor

The I/O pins in SDM bank are supported with weak pull-up and weak pull-down feature. The weak pull-up and weak pull-down feature is pre-configured according to the configuration mode.

Table 29. SDM I/O Internal Weak Pull-Up Resistor

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Min	Typ	Max	Unit
20 kΩ R_{PU}, 20 kΩ R_{PD}	Value of the I/O pin pull-up and pull-down resistor during configuration.	V_{CCIO_SDM} = 1.8 ±5%	15	20	25	kΩ

SDM I/O Hysteresis Specifications for Schmitt Trigger Input

Table 30. SDM I/O Hysteresis Specifications for Schmitt Trigger Input

This device supports Schmitt trigger input on SDM I/O bank. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signal with slow edge rate.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Typ	Max	Unit
V_{HYS}	Hysteresis for Schmitt trigger input	V_{CCIO_SDM} = 1.8 V	180	–	–	mV

I/O Standard Specifications

Tables in this section list the supported input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards.

For minimum voltage values, use the minimum V_{CCIO_PIO} values. For maximum voltage values, use the maximum V_{CCIO_PIO} values.

You must perform timing closure analysis to determine the maximum achievable frequency for general-purpose I/O standards.

(35) This value refers to die-level pin capacitance without the device package.

HSIO I/O Standard Specifications

Related Information

Recommended Operating Conditions on page 14

HSIO Single-Ended I/O Standards Specifications

Table 31. HSIO Single-Ended I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)[36]	V_{OH} (V)[36]
	Min	Typ	Max	Min	Max	Min	Max[37]	Max	Min
1.3 V LVCMOS	1.261	1.3	1.339	–0.3	0.35 × V_{CCIO_PIO}	0.65 × V_{CCIO_PIO}	V_{CCIO_PIO} + 0.25	0.25 × V_{CCIO_PIO}	0.75 × V_{CCIO_PIO}
1.2 V LVCMOS	1.14	1.2	1.26	–0.3	0.35 × V_{CCIO_PIO}	0.65 × V_{CCIO_PIO}	V_{CCIO_PIO} + 0.25	0.25 × V_{CCIO_PIO}	0.75 × V_{CCIO_PIO}
1.1 V LVCMOS	1.045	1.1	1.155	–0.3	0.35 × V_{CCIO_PIO}	0.65 × V_{CCIO_PIO}	V_{CCIO_PIO} + 0.25	0.25 × V_{CCIO_PIO}	0.75 × V_{CCIO_PIO}
1.05 V LVCMOS	0.9975	1.05	1.1025	–0.3	0.35 × V_{CCIO_PIO}	0.65 × V_{CCIO_PIO}	V_{CCIO_PIO} + 0.25	0.25 × V_{CCIO_PIO}	0.75 × V_{CCIO_PIO}
1.0 V LVCMOS	0.95	1	1.05	–0.3	0.35 × V_{CCIO_PIO}	0.65 × V_{CCIO_PIO}	V_{CCIO_PIO} + 0.25	0.25 × V_{CCIO_PIO}	0.75 × V_{CCIO_PIO}

(36) Applicable to test condition of I_{OH} and I_{OL} at 2 mA.

(37) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the $V_{IH(max)}$ for the LVCMOS input can go up to V_{CCIO_PIO} + 0.3 V.

HSIO Single-Ended SSTL, HSTL, HSUL, and POD I/O Reference Voltage Specifications

Table 32. HSIO Single-Ended SSTL, HSTL, HSUL, POD, and LVSTL I/O Reference Voltage Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			Internal V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-12	1.14	1.2	1.26	0.49 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.51 × V_{CCIO_PIO}	0.45 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.55 × V_{CCIO_PIO}
HSTL-12	1.14	1.2	1.26	0.47 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.53 × V_{CCIO_PIO}	0.45 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.55 × V_{CCIO_PIO}
HSUL-12[38]	1.14	1.2	1.26	0.49 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.51 × V_{CCIO_PIO}	0.45 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.55 × V_{CCIO_PIO}
POD12 (GPIO)[39] [40]	1.164	1.2	1.236	0.69 × V_{CCIO_PIO}	0.7 × V_{CCIO_PIO}	0.71 × V_{CCIO_PIO}	—	V_{CCIO_PIO}	—
POD12 (PHYLITE)[39] [40]	1.164	1.2	1.236	0.74 × V_{CCIO_PIO}	0.75 × V_{CCIO_PIO}	0.76 × V_{CCIO_PIO}	—	V_{CCIO_PIO}	—
POD11 (GPIO)[39] [40]	1.067	1.1	1.133	0.69 × V_{CCIO_PIO}	0.7 × V_{CCIO_PIO}	0.71 × V_{CCIO_PIO}	—	V_{CCIO_PIO}	—

continued...

(38) Usage of on-board receiver termination is optional.

(39) Each sub-bank can only support a single voltage tolerance. The V_{CCIO_PIO} tolerance can be extended to ±5% if the entire HSIO sub-bank is operating in any of the following modes. Else, you must supply the V_{CCIO_PIO} voltage rail with a ±3% voltage supply tolerance.
- PHYLITE mode
- GPIO mode

(40) For I/O lane with mixture of GPIO and PHYLITE interfaces, the V_{REF} specification for that I/O lane follows the PHYLITE V_{REF} specifications.

I/O Standard	V_{CCIO_PIO} (V)			Internal V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
POD11 (PHYLITE)[39] [40]	1.067	1.1	1.133	0.74 × V_{CCIO_PIO}	0.75 × V_{CCIO_PIO}	0.76 × V_{CCIO_PIO}	—	V_{CCIO_PIO}	—
LVSTL11[39]	1.067	1.1	1.133	0.24 × V_{CCIO_PIO}	0.25 × V_{CCIO_PIO}	0.26 × V_{CCIO_PIO}	—	GND	—
LVSTL105[39]	1.0185	1.05	1.0815	0.24 × V_{CCIO_PIO}	0.25 × V_{CCIO_PIO}	0.26 × V_{CCIO_PIO}	—	GND	—

HSIO Single-Ended SSTL, HSTL, HSUL, and POD I/O Standards Signal Specifications

Table 33. HSIO Single-Ended SSTL, HSTL, HSUL, and POD I/O Standards Signal Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	$V_{IL(DC)}$ (V)	$V_{IH(DC)}$ (V)	$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)
	Max	Min	Max	Min
SSTL-12	V_{REF} – 0.075	V_{REF} + 0.075	V_{REF} – 0.100	V_{REF} + 0.100
HSTL-12	V_{REF} – 0.080	V_{REF} + 0.080	V_{REF} – 0.150	V_{REF} + 0.150
HSUL-12	V_{REF} – 0.100	V_{REF} + 0.100	V_{REF} – 0.135	V_{REF} + 0.135
POD12	V_{REF} – 0.055	V_{REF} + 0.055	V_{REF} – 0.070	V_{REF} + 0.070
POD11	V_{REF} – 0.055	V_{REF} + 0.055	V_{REF} – 0.070	V_{REF} + 0.070

Note: For output voltage swing calculation example, refer to the *General-Purpose I/O User Guide* for this device. Differential voltage referenced I/O standard uses two single-ended outputs with second output programmed as inverted.

Note: For eye height position estimation in EMIF interfaces, refer to the *PCB Design Guidelines: Agilex™ 3 FPGAs and SoCs*. The eye mask estimation methodology defined in the *PCB Design Guidelines: Agilex™ 3 FPGAs and SoCs* takes precedence over specifications in *HSIO Single-Ended SSTL, HSTL, HSUL, and POD I/O Standards Signal Specifications* table.

Related Information

- General-Purpose I/O User Guide: Agilex 3 FPGAs and SoCs

- PCB Design Guidelines: Agilex 3 FPGAs and SoCs
  Provides eye mask estimation for EMIF interfaces.

HSIO Single-Ended LVSTL I/O Standards Specifications

Table 34. HSIO Single-Ended LVSTL I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			$V_{IL(DC)}$ (V)	$V_{IH(DC)}$ (V)	$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)
	Min	Typ	Max	Max	Min	Max	Min
LVSTL11[41]	1.067	1.1	1.133	V_{REF} – 0.055	V_{REF} + 0.055	V_{REF} – 0.070	V_{REF} + 0.070
LVSTL105[41]	1.0185	1.05	1.0815	V_{REF} – 0.055	V_{REF} + 0.055	V_{REF} – 0.070	V_{REF} + 0.070

Note: For eye height position estimation in EMIF interfaces, refer to the PCB Design Guidelines: Agilex™ 3 FPGAs and SoCs. The eye mask estimation methodology defined in the PCB Design Guidelines: Agilex™ 3 FPGAs and SoCs takes precedence over specifications in HSIO Single-Ended LVSTL I/O Standards Specifications table.

Related Information

PCB Design Guidelines: Agilex 3 FPGAs and SoCs
Provides eye mask estimation for EMIF interfaces.

(41) Each sub-bank can only support a single voltage tolerance. The V_{CCIO_PIO} tolerance can be extended to ±5% if the entire HSIO sub-bank is operating in any of the following modes. Else, you must supply the V_{CCIO_PIO} voltage rail with a ±3% voltage supply tolerance.
- PHYLITE mode
- GPIO mode

HSIO Differential SSTL, HSTL, and HSUL I/O Standards Specifications

Table 35. HSIO Differential SSTL, HSTL, and HSUL I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			$V_{ILdiff(DC)}$ (V)	$V_{IHdiff(DC)}$ (V)	$V_{ILdiff(AC)}$ (V)	$V_{IHdiff(AC)}$ (V)	$V_{IX(AC)}$ (V)			$V_{OX(AC)}$ (V)		
	Min	Typ	Max	Max	Min	Max	Min	Min	Typ	Max	Min	Typ	Max
SSTL-12[42]	1.14	1.2	1.26	–0.15	0.15	–0.2	0.2	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12
HSTL-12[42]	1.14	1.2	1.26	–0.16	0.16	–0.3	0.3	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12
HSUL-12[42]	1.14	1.2	1.26	–0.2	0.2	–0.27	0.27	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12

HSIO Differential POD I/O Standards Specifications

Table 36. HSIO Differential POD I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			$V_{ILdiff(DC)}$ (V)	$V_{IHdiff(DC)}$ (V)	$V_{ILdiff(AC)}$ (V)	$V_{IHdiff(AC)}$ (V)	$V_{IX(AC)}$ (%)[43]
	Min	Typ	Max	Max	Min	Max	Min	Max
POD12[44]	1.164	1.2	1.236	–0.11	0.11	–0.14	0.14	25
POD11[44]	1.067	1.1	1.133	–0.11	0.11	–0.14	0.14	25

(42) Each sub-bank can only support a single voltage tolerance. The V_{CCIO_PIO} tolerance can be extended to ±5% if the entire HSIO sub-bank is operating in any of the following modes. Else, you must supply the V_{CCIO_PIO} voltage rail with a ±3% voltage supply tolerance.
- PHYLITE mode
- GPIO mode

(43) Percentage of P-leg and N-leg crossing relative to the midpoint of P-leg and N-leg signal swings.

Note: For eye height position estimation in EMIF interfaces, refer to the *PCB Design Guidelines: Agilex™ 3 FPGAs and SoCs*. The eye mask estimation methodology defined in the *PCB Design Guidelines: Agilex™ 3 FPGAs and SoCs* takes precedence over specifications in *HSIO Differential POD I/O Standards Specifications* table.

Related Information

PCB Design Guidelines: Agilex 3 FPGAs and SoCs
Provides eye mask estimation for EMIF interfaces.

HSIO Differential LVSTL I/O Standards Specifications

Table 37. HSIO Differential LVSTL I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			$V_{ILdiff(DC)}$ (V)	$V_{IHdiff(DC)}$ (V)	$V_{ILdiff(AC)}$ (V)	$V_{IHdiff(AC)}$ (V)	$V_{IX(AC)}$ (%)(45)
	Min	Typ	Max	Max	Min	Max	Min	Max
LVSTL11(46)	1.067	1.1	1.133	–0.11	0.11	–0.14	0.14	25
LVSTL105(46)	1.0185	1.05	1.0815	–0.11	0.11	–0.14	0.14	25

Note: For eye height position estimation in EMIF interfaces, refer to the PCB Design Guidelines: Agilex™ 3 FPGAs and SoCs. The eye mask estimation methodology defined in the PCB Design Guidelines: Agilex™ 3 FPGAs and SoCs takes precedence over specifications in HSIO Differential LVSTL I/O Standards Specifications table.

(44) Each sub-bank can only support a single voltage tolerance. The V_{CCIO_PIO} tolerance can be extended to ±5% if the entire HSIO sub-bank is operating in any of the following modes. Else, you must supply the V_{CCIO_PIO} voltage rail with a ±3% voltage supply tolerance.
- PHYLITE mode
- GPIO mode

(45) Percentage of P-leg and N-leg crossing relative to the midpoint of P-leg and N-leg signal swings.

(46) Each sub-bank can only support a single voltage tolerance. The V_{CCIO_PIO} tolerance can be extended to ±5% if the entire HSIO sub-bank is operating in any of the following modes. Else, you must supply the V_{CCIO_PIO} voltage rail with a ±3% voltage supply tolerance.
- PHYLITE mode
- GPIO mode

Related Information

PCB Design Guidelines: Agilex 3 FPGAs and SoCs
Provides eye mask estimation for EMIF interfaces.

HSIO Differential I/O Standards Specifications

Table 38. HSIO Differential I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			V_{ID} (mV)		$V_{ICM(DC)}$ (V)			V_{OD} (mV) (47)			V_{OCM} (V)(47)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
True Differential Signaling -1.3 V (LVDS compatible Transmitter and	1.261	1.3	1.339	100	500	0.5	—	1.4(51)	247	—	454	0.9	1	1.1

continued...

(47) R_L range: $90 \leq R_L \leq 110\ \Omega$.

I/O Standard	V_{CCIO_PIO} (V)			V_{ID} (mV)		$V_{ICM(DC)}$ (V)			V_{OD} (mV) (47)			V_{OCM} (V)(47)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
Receiver) (48) (49) (50)														
True Differential Signaling -1.2 V (Receiver only)(48)	1.14	1.2	1.26	100	454	0.8	—	0.95	—	—	—	—	—	—
True Differential Signaling -1.1 V (Receiver only)(48)	1.045	1.1	1.155	100	454	0.8	—	0.95	—	—	—	—	—	—

continued...

(47) R_L range: $90 \leq R_L \leq 110\ \Omega$.

I/O Standard	V_{CCIO_PIO} (V)			V_{ID} (mV)		$V_{ICM(DC)}$ (V)			V_{OD} (mV) (47)			V_{OCM} (V)(47)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
True Differential Signaling -1.05 V (Receiver only)(48)	0.9975	1.05	1.1025	100	454	0.8	—	0.95	—	—	—	—	—	—
SLVS400	1.164	1.2	1.236	70	—	0.07	0.2	0.33	—	—	—	—	—	—
	1.067	1.1	1.133											

Related Information

- General-Purpose I/O User Guide: Agilex™ 5 FPGAs and SoCs
- LVDS SERDES User Guide: Agilex™ 5 FPGAs and SoCs
- AN 555: True Differential Signaling Termination and Biasing for Agilex™ 7 M-Series, Agilex™ 5, and Agilex™ 3 FPGAs

(47) R_L range: $90 \leq R_L \leq 110\ \Omega$.

(48) The True Differential Signaling input buffer is supported on 1.05 V, 1.1 V, 1.2 V, and 1.3 V V_{CCIO_PIO} banks. The maximum input voltage driven into the True Differential Signaling input buffer must not exceed $V_{ICM(max)} + V_{ID(max)}/2$.

(49) True Differential Signaling - 1.3 V standard is compatible with LVDS and capable to interface with LVDS subsets such as:
- RSDS
- Mini-LVDS
- Any I/O standards using equivalent electrical specifications

(50) For further information on True Differential Signaling - 1.3 V feature support and guidelines on interfacing True Differential Signaling -1.3V standard with LVDS and its subset compliant standards, refer to the related information.

(51) The $V_{ICM(DC)}$ voltage must not exceed 1.2 V when on-chip differential termination (R_D OCT) is disabled with the use of external on-board termination.

MIPI D-PHY I/O Standards Specifications

Table 39. Agilex 3 FPGAs MIPI D-PHY Low-Power I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	Condition	V_{CCIO_PIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OH} (V)			V_{OL} (V)		
		Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
DPHY	Applicable for low power when the supported High-Speed data rate 150 Mbps to 2.5 Gbps	1.164	1.2	1.236	—	0.55	0.74	—	1.1	1.2	1.3	–0.05	—	0.05
	Applicable for low power when the supported High-Speed data rate 150 Mbps to 2.5 Gbps	1.067	1.1	1.133					0.95(52)	1.1(52)	1.2(52)			

(52) Receivers compliant to D-PHY v2.1 and later supports a V_{IH} compatible with V_{OH} level regardless of the supported High-Speed data rate.

Table 40. Agilex 3 FPGAs MIPI D-PHY High-Speed I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	Condition	V_{CCIO_PIO} (V)			V_{ID} (V)		$V_{ICM(DC)}$ (V)			$V_{OD(DC)}$ (V)			V_{OCM} (V)			V_{ILHS} (V)	V_{IHHS} (V)
		Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
DPHY	Data rate ≤ 1.5 Gbps	1.164	1.2	1.236	0.07	—	0.07	—	0.33	0.14	0.2	0.27	0.15	0.2	0.25	–0.04	0.46
	Data rate > 1.5 Gbps to 2.5 Gbps				0.04												
	Data rate ≤ 1.5 Gbps	1.067	1.1	1.133	0.07												
	Data rate > 1.5 Gbps to 2.5 Gbps				0.04												

HVIO I/O Standard Specifications

Related Information

Recommended Operating Conditions on page 14

HVIO Single-Ended I/O Standards Specifications

Table 41. HVIO Single-Ended I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_HVIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)(53)	V_{OH} (V)(53)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min
1.8 V LVCMOS 1.8 V LVTTL	1.746	1.8	1.854	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45
2.5 V LVCMOS 2.5 V LVTTL	2.425	2.5	2.575	-0.3	0.7	1.7	V_{CCIO} + 0.3	0.4	2
3.3 V LVCMOS 3.3 V LVTTL	3.201	3.3	3.399	–0.3	0.8	2	V_{CCIO} + 0.3	0.4	2.4

HPS I/O Standard Specifications

Tables in this section list the supported input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards.

For minimum voltage values, use the minimum V_{CCIO_HPS} values. For maximum voltage values, use the maximum V_{CCIO_HPS} values.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

(53) Applicable to test condition of I_{OH} and I_{OL} at 3 mA.

HPS Single-Ended I/O Standards Specifications

Table 42. HPS Single-Ended I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_HPS}			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)(54)	I_{OH} (mA)(54)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min	Max	Min
1.8 V LVCMOS	1.71	1.8	1.89	–0.3	0.35 × V_{CCIO_HPS}	0.65 × V_{CCIO_HPS}	V_{CCIO_HPS} + 0.3	0.4	V_{CCIO_HPS} – 0.4	8	–8

SDM I/O Standard Specifications

Tables in this section list the supported input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards.

For minimum voltage values, use the minimum V_{CCIO_SDM} values. For maximum voltage values, use the maximum V_{CCIO_SDM} values.

SDM Single-Ended I/O Standards Specifications

Table 43. SDM Single-Ended I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_SDM} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)(55)	I_{OH} (mA)(55)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min	Max	Min
1.8 V LVCMOS	1.71	1.8	1.89	–0.3	0.35 × V_{CCIO_SDM}	0.65 × V_{CCIO_SDM}	V_{CCIO_SDM} + 0.3	0.4	V_{CCIO_SDM} – 0.4	8	–8

(54) To meet the I_{OH} and I_{OL} specifications, you must set the current strength settings accordingly. For example, to meet the 1.8 V LVCMOS specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OH} and I_{OL} specifications in the data sheet.

(55) To meet the I_{OH} and I_{OL} specifications, you must verify the current strength settings accordingly. For example, to meet the 1.8 V LVCMOS specification (8 mA), you should verify the current strength settings used is 8 mA . Using a lower current strength may not meet the I_{OH} and I_{OL} specifications in the data sheet.

Switching Characteristics

This section provides the performance characteristics of core and periphery blocks.

Core Performance Specifications

Clock Tree Specifications

Table 44. Agilex 3 FPGAs Clock Tree Performance Specifications

For specification status, see the *Data Sheet Status* table

Parameter	Performance		Unit
	–6S	–7S	
Programmable clock routing	710	554	MHz

I/O PLL Specifications

Table 45. Agilex 3 FPGAs I/O PLL Specifications

For specification status, see the *Data Sheet Status* table

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN}	Input clock frequency source from reference clock input	–6S	10	—	900[56]	MHz
		–7S	10	—	625[56]	MHz
	Input clock frequency source from core clock input	–6S	10	—	415[56]	MHz
		–7S	10	—	353[56]	MHz
	Input clock frequency source from HSIO clock input	–6S	10	—	717[56]	MHz
		–7S	10	—	625[56]	MHz

continued...

(56) This specification is limited by the I/O maximum frequency. The maximum achievable I/O frequency is different for each I/O standard and is dependent on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	Input clock frequency source from HVIO clock input	—	10	—	156.25[56]	MHz
f_{INPFD}	Input clock frequency to the PFD	—	10	—	325	MHz
f_{VCO}	I/O PLL VCO operating range	–6S	600	—	3,200	MHz
		–7S	600	—	2,400	MHz
f_{CLBW}	I/O PLL closed-loop bandwidth	—	0.5	—	20	MHz
f_{OUT}	Output frequency for internal clock (C counter)	–6S	—	—	1,000	MHz
		–7S	—	—	780	MHz
f_{OUT_EXT}	Output frequency for external clock output	–6S	—	—	717	MHz
		–7S	—	—	625	MHz
$t_{OUTDUTY}$	Duty cycle for dedicated external clock output (when set to 50%)	f_{OUT_EXT} < 300 MHz	45	50	55	%
		f_{OUT_EXT} ≥ 300 MHz	40/45 [57]	50	55 [57]/60	%
t_{FCOMP} [58]	External feedback clock compensation time	—	—	—	5	ns
$f_{DYCONFIGCLK}$	Dynamic configuration clock	—	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of areset	—	—	—	1	ms

continued...

(57) To achieve 5% duty cycle for f_{OUT_EXT} ≥ 300 MHz, you only can use `tx_outclk` port from the LVDS SERDES FPGA IP. Refer to the *Clocking and PLL User Guide* for the detail design guidelines.

(58) Not applicable for fabric-feeding I/O PLL.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/ delays)	—	—	—	1	ms
t_{PLL_PSERR} (59)	Accuracy of PLL phase shift	—	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the areset signal	—	10	—	—	ns
t_{INCCJ}	Input clock cycle-to-cycle jitter	f_{REF} < 100 MHz (60)	—	—	±750	ps (p-p)
		f_{REF} ≥ 100 MHz (60)	—	—	0.15	UI (p-p)
t_{REFPJ}	Reference phase jitter (rms)(61)	Carrier frequency: 100 MHz with integrated bandwidth of 10 kHz to 50 MHz	—	—	1.42	ps
t_{REFPN}	Reference phase noise(62) (61)	10 Hz	—	—	–90	dBc/Hz
		100 Hz	—	—	–100	dBc/Hz
		1 kHz	—	—	–110	dBc/Hz
		10 kHz	—	—	–120	dBc/Hz
		100 kHz	—	—	–130	dBc/Hz
		1 MHz	—	—	–138	dBc/Hz

continued...

(59) PLL phase shift accuracy is 50 ps with the assumption of f_{VCO} = 1.6 GHz.

(60) f_{REF} is f_{IN}/N, specification applies when N = 1.

(61) Requirement for DDR/LPDDR protocol and LVDS SERDES applications only.

(62) The phase noise numbers in this table are the maximum acceptable phase noise values measured at a carrier frequency of 100 MHz. To calculate the phase noise requirement at any other frequency, use the formula: `REFCLK` phase noise at f (MHz) = `REFCLK` phase noise at 100 MHz + (20 × log10 (f/100)).

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		10 MHz	—	—	–142	dBc/Hz
		100 MHz	—	—	–144	dBc/Hz
t_{OUTPJ_DC} (58) (63)	Period jitter for dedicated clock output	f_{OUT} < 100 MHz (60)	—	—	17.5	mUI (p-p)
		f_{OUT} ≥ 100 MHz (60)	—	—	175	ps (p-p)
t_{OUTCCJ_DC} (58) (63)	Cycle-to-cycle jitter for dedicated clock output	f_{OUT} < 100 MHz (60)	—	—	17.5	mUI (p-p)
		f_{OUT} ≥ 100 MHz (60)	—	—	175	ps (p-p)
t_{OUTPJ_IO} (64) (63)	Period jitter for clock output on the regular I/O	f_{OUT} < 100 MHz (60)	—	—	60	mUI (p-p)
		f_{OUT} ≥ 100 MHz (60)	—	—	600	ps (p-p)
t_{OUTCCJ_IO} (64) (63)	Cycle-to-cycle jitter for clock output on the regular I/O	f_{OUT} < 100 MHz (60)	—	—	60	mUI (p-p)
		f_{OUT} ≥ 100 MHz (60)	—	—	600	ps (p-p)
$t_{CASC\_OUTPJ\_DC}$ (58)	Period jitter for dedicated clock output in cascaded PLLs	f_{OUT} < 100 MHz (60)	—	—	17.5	mUI (p-p)
		f_{OUT} ≥ 100 MHz (60)	—	—	175	ps (p-p)
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	f_{IN} ≥ 600 MHz	30	—	70	%
		450 MHz ≤ f_{IN} < 600 MHz	35	—	65	%
		250 MHz ≤ f_{IN} < 450 MHz	40	—	60	%
		10 MHz ≤ f_{IN} < 250 MHz	45	—	55	%

(63) This jitter specification does not include the effect of spread-spectrum clock. The magnitude of jitter deterioration is largely depend on the spread-spectrum clock profile used. Refer to the *Clocking and PLL User Guide* for the recommended spread-spectrum clock profile.

(64) External memory interface clock output jitter specifications use a different measurement method, which are available in the *Memory Output clock Jitter Specifications* table.

Related Information

Memory Output Clock Jitter Specifications on page 59
Provides more information about the external memory interface clock output jitter specifications.

DSP Block Specifications

Table 46. Agilex 3 FPGAs DSP Block Performance Specifications for Single DSP Block

For specification status, see the *Data Sheet Status* table

Mode	Performance		Unit
	-6S	-7S	
Fixed-point 18 × 19 multiplication mode	415	353	MHz
Fixed-point 27 × 27 multiplication mode	415	353	MHz
Fixed-point 18 × 19 multiplier adder mode	415	353	MHz
Fixed-point 18 × 19 multiplier adder summed with 36-bit input mode	415	353	MHz
Fixed-point six 9 × 9 multiplier adder mode	415	353	MHz
FP32 floating-point multiplication mode	367	306	MHz
FP32 floating-point adder or subtract mode	367	306	MHz
FP32 floating-point multiplier adder or subtract mode	367	306	MHz
FP32 floating-point multiplier accumulate mode	367	306	MHz
Addition or subtraction of two FP16 floating-point multiplication mode	367	306	MHz
Sum/sub of two FP16 multiplications with FP32 (addition/subtraction)	367	306	MHz
Sum/sub of two FP16 multiplications with accumulation (addition/subtraction)	367	306	MHz

continued...

Mode	Performance		Unit
	-6S	-7S	
Tensor floating-point mode	367	306	MHz
Tensor accumulation mode: fp32	367	306	MHz
Tensor fixed-point mode	415	353	MHz
INT16 complex multiplication mode	415	353	MHz

Table 47. Agilex 3 FPGAs DSP Block Performance Specifications for Multiple DSP Blocks

For specification status, see the *Data Sheet Status* table

Mode	Performance		Unit
	-6S	-7S	
Fixed-point 18 x 19 complex multiplication mode	415	353	MHz
Fixed-point 18 × 19 FIR systolic mode	415	353	MHz
Fixed-point 27 × 27 multiplication mode	367	306	MHz
Fixed-point 9 × 9 multiplication mode	367	306	MHz
FP32 floating-point complex multiplication	367	306	MHz
FP32 floating-point vector dot product	367	306	MHz
FP16 floating-point complex multiplication	367	306	MHz
FP16 floating-point vector dot product	367	306	MHz
Tensor floating-point cascade chain	367	306	MHz
Tensor fixed-point cascade chain	415	353	MHz

Memory Block Specifications

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL and set to 50% output duty cycle. Use the Quartus Prime software to report timing for the memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in f_{MAX}.

Table 48. Agilex 3 FPGAs Memory Block Performance Specifications

For specification status, see the *Data Sheet Status* table

Memory	Mode	Performance		Unit
		–6S	–7S	
MLAB	Single-port RAM/ROM Simple dual-port RAM	415	353	MHz
	Simple dual-port RAM with read-during-write option set to New Data or Old Data	310	280	MHz
M20K block[65]	Single-port RAM/ROM Simple dual-port RAM	415	353	MHz
	Simple dual-port RAM, coherent read enabled	415	353	MHz
	Single-port RAM with the read-during-write option set to Old Data Simple dual-port RAM with the read-during-write option set to Old Data	415	353	MHz
	Simple dual-port RAM with ECC enabled, 512 × 32	330	280	MHz
	Simple dual-port RAM with ECC, optional pipeline registers enabled, 512 × 32	415	353	MHz
	Dual-port ROM True dual-port RAM	335	280	MHz
	Simple quad-port RAM	335	280	MHz

(65) For the M20K block, Quartus automatically optimizes timing and power based on design requirements.

Local Temperature Sensor Specifications

Table 49. Local Temperature Sensor Specifications

For specification status, see the *Data Sheet Status* table

Description	Temperature Range	Accuracy	Sampling Rate[66]	Conversion Time
Local temperature sensor	–40 to 125°C[67]	±5°C	1 KSPS	< 1 ms

Related Information

Recommended Operating Conditions on page 14

Remote Temperature Diode Specifications

Note the following for the remote temperature diode specifications:

- The temperature diode characteristics in this table target for three-currents temperature sensing chip implementation. The characteristics can also apply to two-currents temperature sensing chip implementation.
- Absolute accuracy is dependent on third-party external diode ADC and integration specifics.

Table 50. Remote Temperature Diode Specifications (Core Fabric TSD)

For specification status, see the *Data Sheet Status* table

Description	Min	Typ	Max	Unit
I_{bias}, diode source current	30	—	170	µA
V_{bias}, voltage across diode	0.51	—	0.82	V
Series resistance	—	—	<5	Ω
Diode ideality factor	—	1.005[68]	—	—

(66) The read out is subject to the SDM mailbox activity status.

(67) Temperature range refers to junction temperature.

(68) When using lower injection current (two-currents) implementation, the ideality factor is 1.014.

Voltage Sensor Specifications

Table 51. Voltage Sensor Specifications

For specification status, see the *Data Sheet Status* table

Parameter		Minimum	Typical	Maximum	Unit
Resolution		—	7	—	Bit
Sampling rate[69]		—	—	1	KSPS
Input capacitance		—	—	40	pF
External reference voltage		1.125	1.25	1.375	V
Voltage sensor accuracy, V_{in} range: 0 V to 1.1 V[70] [71]		—	—	±3.5	%
Unipolar input mode	Input signal range for Vsigp	—	—	1.35	V
	Common mode voltage on Vsign	—	—	0.25	V
	Input signal range for Vsigp – Vsign	—	—	1.1	V

Periphery Performance Specifications

This section describes the periphery performance, LVDS SERDES, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

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(69) The read out is subject to the SDM mailbox activity status.

(70) For low voltage channel in channel 0, 1, 2, 6, and 7, the ±3.5% accuracy equals to ±43.75mV. For high voltage channels in channel 3, 4, 5, and 9, the accuracy is ±4.5%. This equals to ±56.25mV.

(71) When Voltage Tamper Detection is enabled, the voltage sensor accuracy specifications are as follows:
- For low voltage channel in channel 0, 1, 2, 6, and 7, the accuracy is ±5.5%. This equals to ±68.75mV.
- For high voltage channels in channel 3, 4, 5, and 9, the accuracy is ±6.5%. This equals to ±81.25mV.

LVDS SERDES Specifications

Table 52. Agilex 3 FPGAs LVDS SERDES Specifications

LVDS serializer/deserializer (SERDES) block supports SERDES factor J = 4 and 8.

DDR registers support SERDES factor J = 1 and 2.

You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

For specification status, see the *Data Sheet Status* table

Parameter	Symbol	Condition	–6 Speed Grade			–7 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	
Clock frequency	f_{HSCLK_in} (input clock frequency) True Differential Signaling I/O Standards	Clock boost factor W = 1 to 40[72]	10	—	625	10	—	500	MHz
	f_{HSCLK_in} (input clock frequency) SLVS400 I/O Standards	Clock boost factor W = 1 to 40[72]	10	—	445.5	10	—	445.5	MHz
	f_{HSCLK_in} (input clock frequency) Single-Ended I/O Standards	Clock boost factor W = 1 to 40[72]	10	—	625	10	—	525	MHz
	f_{HSCLK_OUT} (output clock frequency) True	—	—	—	625	—	—	500	MHz

continued...

(72) Clock Boost Factor (W) is the ratio between the input data rate and the input clock rate.

Parameter	Symbol	Condition	–6 Speed Grade			–7 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	
	Differential Signaling I/O Standards								
Transmitter	True Differential Signaling I/O Standards - f_{HSDR} (data rate)[73]	SERDES factor J = 4 and 8[74] [75] [76]	600	—	1,250	600	—	1,000	Mbps
		SERDES factor J = 2, uses DDR registers	[76]	—	500[77]	[76]	—	500[77]	Mbps
		SERDES factor J = 1, uses DDR registers	[76]	—	250[77]	[76]	—	250[77]	Mbps
	t_x Jitter - True Differential Signaling I/O Standards	Total jitter for data rate, 600 Mbps – 1.25 Gbps	≤1,250 Mbps: 160 ≤1,000 Mbps: 180 ≤800 Mbps: 210 600 Mbps: 240			≤1,000 Mbps: 180 ≤800 Mbps: 210 600 Mbps: 240			ps
	t_{DUTY} [78]	TX output clock duty cycle for True	45	50	55	45	50	55	%

continued...

(73) Requires package skew compensation with PCB trace length.

(74) The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

(75) The V_{CC} and V_{CCP} must be on a combined power layer and a maximum load of 5 pF for chip-to-chip interface.

(76) The minimum specification depends on the following factors. The differential I/O buffer within the IOE does not have a minimum data rate.

(77) You must perform design timing analysis in Quartus Prime to achieve timing closure and run IBIS/HSPICE simulations to ensure that the I/O buffer's electrical performance meets the interface requirements.

(78) Not applicable for DIVCLK = 1.

Parameter	Symbol	Condition	–6 Speed Grade			–7 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	
		Differential Signaling I/O Standards							
	t_{RISE} and t_{FALL} (75) (79)	True Differential Signaling I/O Standards	—	—	160	—	—	200	ps
	T_{CCS} (73) (78)	True Differential Signaling I/O Standards	—	—	202	—	—	202	ps
Receiver(80)	True Differential Signaling I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 4 and 8(74) (75) (76)	600	—	1250(81)	600	—	1000(81)	Mbps
	SLVS400 I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 4 and 8(74) (75) (76)	600	—	891	600	—	891	Mbps
	f_{HSDR} (data rate) (without DPA)(73)	SERDES factor J = 4 and 8(74) (75) (76)	150	—	(82)	150	—	(82)	Mbps

continued...

(79) This applies to default pre-emphasis and V_{OD} settings only.

(80) When operating in DPA mode, you must enable the receiver equalization feature of the input buffer.

(81) 1.05 V, 1.1 V, and 1.2 V True Differential Signaling I/O standards on receiver supports data rate up to 1000 Mbps.

(82) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

Parameter	Symbol	Condition	–6 Speed Grade			–7 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	
		SERDES factor J = 2, uses DDR registers	(76)	—	500(77)	(76)	—	500(77)	Mbps
		SERDES factor J = 1, uses DDR registers	(76)	—	250(77)	(76)	—	250(77)	Mbps
DPA (FIFO mode)	DPA run length	—	—	—	≤10,000	—	—	≤10,000	UI
DPA (soft CDR mode)	DPA run length	SGMII/GbE protocol	—	—	5	—	—	5	UI
		All other protocols	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—
Soft CDR mode	Soft-CDR ppm tolerance	—	–300	—	300	–300	—	300	ppm
Non DPA mode	Sampling window	—	—	—	330	—	—	330	ps

DPA Lock Time Specifications

Table 53. DPA Lock Time Specifications

The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1-to-0 transition.

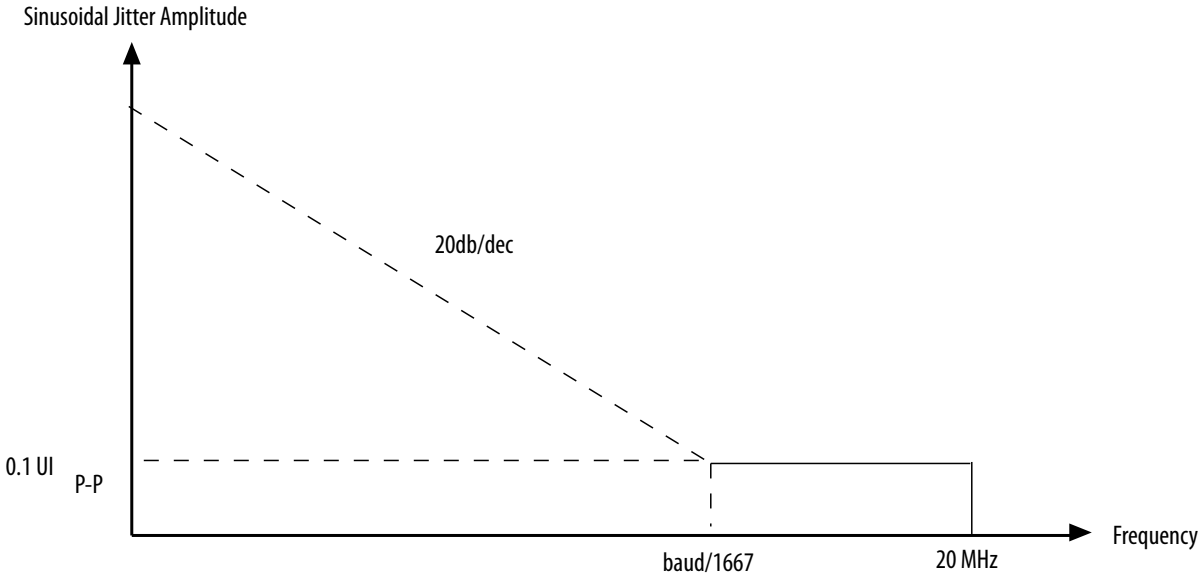
For specification status, see the *Data Sheet Status* table

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions(83)	Maximum Data Transition
SPI-4	00000000001111111111	2	128	768
Parallel Rapid I/O	00001111	2	128	768
	10010000	4	64	768
Miscellaneous	10101010	8	32	768
	01010101	8	32	768

(83) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

LVDS SERDES Soft-CDR Sinusoidal Jitter Tolerance Specifications

Figure 2. LVDS SERDES Soft-CDR Sinusoidal Jitter Tolerance Specifications for a Data Rate Less than or Equal to 1.25 Gbps



Memory Standards Supported

Table 54. Agilex 3 FPGAs Memory Standards Supported

This table lists the overall capability of External Memory Interface supported by Agilex 3 FPGAs. For specific details, refer to the *External Memory Interface Spec Estimator*.

For specification status, see the *Data Sheet Status* table

Memory Standard	Controller Type	Maximum Frequency (MHz)
LPDDR4 SDRAM	Hard memory controller	1,067
LPDDR4 SDRAM	HPS hard memory controller	1,067

Related Information

External Memory Interface (EMIF) Spec Estimator

Memory Output Clock Jitter Specifications

The clock jitter specification applies to the memory output clock pins clocked by an I/O PLL, or generated using double data I/O circuits clocked by a PLL output routed on a PHY clock network as specified. Altera recommends using PHY clock networks for better jitter performance.

The memory clock output jitter is within the JEDEC* specifications when the phase jitter (integration bandwidth 10 kHz to 50 MHz) of the input clock is not more than 20 ps peak-to-peak, or 1.42 ps RMS at $1e^{-12}$ BER and 1.22 ps at $1e^{-16}$ BER.

MIPI D-PHY Performance

Table 55. Agilex 3 FPGAs MIPI D-PHY Performance

For specification status, see the *Data Sheet Status* table

Parameter	Symbol	Condition	–6Speed Grade			–7 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	
MIPI D-PHY transmitter or receiver	High-speed interface, Hs	Short reference, standard reference, or long reference (84)	150	—	2,500	150	—	2,500	Mbps
	Low-power interface, Lp	—	—	—	20	—	—	20	MHz

(84) The long reference/standard reference/short reference is reference to the insertion loss condition from MIPI Alliance D-PHY specifications.

GTS Transceiver Performance Specifications

GTS Transceiver Performance

Table 56. Transmitter and Receiver Data Rate Performance

For specification status, see the *Data Sheet Status* table

Symbol/Description	Transceiver Speed	Unit
Supported data rate for Agilex 3 (NRZ)	1 – 12.5	Gbps

GTS Transceiver Reference Clock Specifications

Table 57. GTS Transceiver and System PLL Reference Clock Input Specifications

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Typical	Max	Unit
—	Supported I/O standards	Dedicated reference clock pin	CML, HCSL			
F_{REF}	Reference clock operating frequency	—	100(85)	—	380	MHz
$T_{REF-DUTY}$	Duty cycle	—	45	50	55	%
$T_{REF-RISE/FALL}$	Rise and fall time (as percentage of period)	20% – 80%	—	—	0.15	T_{REF}
SSC	Spread-spectrum downspread	PCIe*	—	–5,000 to 0	—	ppm
$T_{REF-SINGLEEND-SKEW}$	Skew between `REFCLKP` and `REFCLKN`	—	—	—	50	ps
$Z_{REF-DIFF-DC}$	Reference clock differential input impedance – terminated mode	—	80	100	120	Ω

continued...

(85) This value is 100 MHz for down spread spectrum clocking (SSC). This value can also be 25 MHz for HDMI rate of less than 1 Gbps.

Symbol	Description	Condition	Min	Typical	Max	Unit
$V_{min-ABS}$	Absolute V_{min}	—	–0.15	—	—	V
$V_{max-ABS}$	Absolute V_{max}	—	—	—	0.85	V
$V_{REFIN-DIFF-AC}$	Input reference clock differential peak-to-peak voltage when AC-coupled on board	—	0.6	1.2	1.7	V
$V_{REFIN-IL-DC}$	Input reference clock input low voltage when DC-coupled on board	—	–0.15	0	0.15	V
$V_{REFIN-IH-DC}$	Input reference clock input high voltage when DC-coupled on board	—	0.66	0.7	0.85	V
$V_{REFIN-CM-AC}$	Input reference clock common-mode voltage when AC-coupled on board	—	Set on chip			V
$V_{REFIN-CM-DC}$	Input reference clock common-mode voltage when DC-coupled on board	—	0.255	0.35	0.5	V
PN_{REF}	Transmitter REFCLK phase noise (156.25 MHz)(86) (85)	10 kHz	—	—	–130	dBc/Hz
		100 kHz	—	—	–138	dBc/Hz
		500 kHz	—	—	–138	dBc/Hz
		3 MHz	—	—	–140	dBc/Hz
		10 MHz	—	—	–144	dBc/Hz
		20 MHz	—	—	–146	dBc/Hz
		1 GHz	—	—	–146	dBc/Hz

continued...

(86) To calculate the REFCLK phase noise requirement at frequencies other than 156.25 MHz, use the following formula: REFCLK phase noise at f (MHz) = REFCLK phase noise at 156.25 MHz + 20 × log(f/156.25 MHz).

Symbol	Description	Condition	Min	Typical	Max	Unit
$V_{REFIN-RJ-RMS}$	RMS jitter integrated from 10 kHz – 20 MHz including spurs	—	—	—	522	fs
$V_{REFIN-PPM-ERROR}$	Reference clock frequency error	—	–350 + SSC	—	+350 + SSC	ppm
R_{COMP}	External resistor for calibration	—	—	499 ± 0.1%	—	Ω

Table 58. System PLL Reference Clock (Using HVIO) Specifications

For specifications on the I/O PLL using HVIO pin, refer to *Agilex 3 FPGAs I/O PLL Specifications*.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Typical	Max	Unit
F_{REF}	Clock input frequency	Powered by V_{CCIO_HVIO}	25	—	125	MHz
$T_{REF-DUTY}$	Clock input duty cycle		45	50	55	%

Table 59. GTS Transceiver Reference Clock Output Driver Specifications

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Typical	Max	Unit
F_{REF_OUT}	Reference clock operating frequency	—	25	—	380	MHz
$T_{REF-DUTY\_OUT}$	Duty cycle	—	45	50	55	%
$T_{REF-RISE\_OUT/FALL\_OUT}$	Rise and fall time (as percentage of period)	20% – 80%	—	—	0.15	T_{REF}
$T_{REF-SINGLEEND-SKEW}$	Skew between `REFCLKP` and `REFCLKN`	—	—	—	50	ps

continued...

Symbol	Description	Condition	Min	Typical	Max	Unit
$Z_{REF-DIFF-DC\_OUT}$	Reference clock differential output impedance – terminated mode	—	80	100	120	Ω
$V_{REF-DIFF-AC\_OUT}$	Output reference clock differential peak to peak voltage when AC-coupled on board	—	0.9	1	1.1	V
$V_{REF-CM-OUT}$	Output reference clock common-mode	—	0.45	0.5	0.55	V

Transmitter Specifications

Table 60. Transmitter Electrical Specifications

For specification status, see the *Data Sheet Status* table

Parameter	Symbol	Description	Condition	Min	Typical	Max	Unit
On-chip termination	—	Transmitter differential on-chip termination resistors	—	80	90	120	Ω
Transmitter output eye specifications	$V_{TX-DIFF-PKPK}$	Back-porch transmit amplitude	—	300	—	1,050	mV
	$V_{TX-DEEMP\_STEP}$	Transmitter tap resolution	—	—	—	2	%
	$D_{TX-PRE\_TAP\_2}$	Pre-cursor tap 2 de-emphasis	—	0	—	2.5	dB
	$D_{TX-PRE\_TAP\_1}$	Pre-cursor tap 1 de-emphasis	—	0	—	4.5	dB
	$D_{TX-POST\_TAP\_1}$	Post-cursor tap 1 de-emphasis	—	0	—	6.5	dB
	$T_{TX-SLEW}$	Rise/fall time at 20%–80%	—	10	—	20	ps

continued...

Parameter	Symbol	Description	Condition	Min	Typical	Max	Unit
	T_{TX-DJ}	Transmitter deterministic jitter at 12.5 Gbps	—	—	—	0.15	UI_{pkpk}
	T_{TX-RJ}	Transmitter total peak-peak random jitter(87)	At BER of 10^{-12}	—	—	0.15	UI_{pkpk}
	T_{TX-TJ}	Transmitter total peak-peak jitter ($T_{TX-TJ} = T_{TX-DDJ} + T_{TX-PJ} + T_{TX-RJ}$)(87)(88)	At BER of 10^{-12}	—	—	0.28	UI_{pkpk}
Transmitter DC impedance	$Z_{TX-DIFF-DC}$	Transmitter output differential DC impedance with OCT 90 Ω mode while configured(89)	—	80	90	120	Ω
	$Z_{TX-CM-DC}$	Transmitter output common-mode DC impedance	—	20	22.5	30	Ω
Transmitter return loss	$Z_{RL-DIFF-DC}$	Transmitter differential DC return loss	—	—	—	–12	dB
	$Z_{RL-DIFF-NYQ}$	Transmitter differential return loss at Nyquist frequency ($F_{BAUD}/2$)	—	—	—	–6	dB

continued...

(87) Assume a 1st order high-pass jitter measurement filter with a cutoff of $F_{BAUD}/F_{GPLL} = N_{GPLL}$, where N_{GPLL} is the ratio of the 3 dB cutoff frequency to the data rate, with typical value of 1,667.

(88) The maximum TJ value is slightly less than the sum of DDJ + PJ + RJ to take into consideration of the worst case probability, where both deterministic and random jitter component might present at the same time.

(89) TX pins are driven to 0 V before configuration.

Parameter	Symbol	Description	Condition	Min	Typical	Max	Unit
	Z_{RL-CMN}	Transmitter common-mode return loss below 10 GHz	—	—	—	–6	dB
Electrical idle	$V_{TX-IDLE}$	Electrical idle output voltage	PCIe/ SATA/SAS/USB	—	—	20	mV
	$V_{CM-DELTA-SQUELCH}$	Maximum common-mode step entering/ exiting squelch mode		—	—	100	mV
	$T_{TX-IDLE-LATENCY}$	Latency entering/ exiting electrical idle		—	—	8	µs
Receiver detect	$V_{TX-RCV-DETECT}$	Receiver detect voltage change allowed during receiver detection	PCIe/ SATA/SAS/USB	—	—	600	mV
Lane-to-lane output skew	—	Lane-to-lane output skew	Lane count ≤ 4	—	—	2 UI + 166 ps	ps

Receiver Specifications

Table 61. Receiver Electrical Specifications

For specification status, see the *Data Sheet Status* table

Parameter	Symbol	Description	Condition	Min	Typical	Max	Unit
On-chip termination	—	Receiver differential on-chip termination resistors	—	65	85	102	Ω
				80	100	120	Ω

continued...

Parameter	Symbol	Description	Condition	Min	Typical	Max	Unit
Receiver input eye specifications	$V_{RX-DIFF-PKPK}$	Receiver input differential peak-to-peak voltage(90)	—	Closed eye(91)	—	1,200	mV
	V_{RX-MAX}	Receiver input maximum voltage(92)	—	—	—	1	V
	V_{RX-MIN}	Receiver input minimum voltage(92)	—	–0.3	—	—	V
	$V_{RX-CM-DC}$	Receiver input DC common-mode voltage(93)	When squelch detector is not enabled	0	—	700	mV
			When squelch detector is enabled	200	—	300	mV
	T_{RX-RJ}	Receiver input random jitter	At BER of 10^{-12}	—	—	0.15	UI_{pkpk}
	T_{RX-PJ}	Receiver input periodic jitter (at high frequency(94))	—	—	—	0.05	UI_{pkpk}
Insertion loss specification	$I_{INS-LOSS-10.3125Gb/s\_BER10-12}$	Insertion loss at Nyquist frequency ($F_{BAUD}/2$)(95)	At BER of 10^{-12}	—	—	-25	dB

continued...

(90) This is supported when the receiver is powered and configured, powered and unconfigured, or unpowered.

(91) Closed eye at the Receiver input buffer can be recovered and opened up with the Agilex 3 Receiver equalizer.

(92) V_{RX_MAX} and V_{RX_MIN} are before and after configuration.

(93) The specified common-mode range is supported when the receiver is powered and configured, powered and unconfigured, or unpowered. This specification is also supported before mode configuration. If squelch detect is used, receiver DC input common-mode voltage should be within 200 mV to 300 mV. Otherwise, use AC coupling capacitors on board.

(94) High frequency is defined as frequencies beyond the CDR loop bandwidth (typically $F_{BAUD}/1,667$).

Parameter	Symbol	Description	Condition	Min	Typical	Max	Unit
Receiver return loss	$Z_{RL-DIFF-DC}$	Receiver differential DC return loss	—	—	—	–12	dB
	$Z_{RL-DIFF-NYQ}$	Receiver differential return loss at Nyquist frequency ($F_{BAUD}/2$)	—	—	—	–6	dB
	Z_{RL-CM}	Receiver common-mode return loss below 10 GHz	—	—	—	–6	dB
Receiver DC impedance	$R_{DIFF-DC}$	Receiver differential DC impedance	85 Ω on-chip termination	65	85	102	Ω
			100 Ω on-chip termination	80	100	120	Ω
	R_{CM-DC}	Receiver common-mode DC impedance	—	20	25	30	Ω
Receiver signal detection[96]	$V_{IDLE-THRESH}$	Receiver signal detect input voltage threshold	—	75	120	175	mV

(95) COM compliant package and channel. Based on 10GKR compliance testing at 10.3125 Gbps.

(96) Receiver signal detection values in this table are applicable to PCIe and similar standards, such as SATA, where a clock pattern like PCIe EIEOS 500 MHz clock pattern is used.

Electrical Compliance

Table 62. Electrical Compliance List

For specification status, see the *Data Sheet Status* table

Specification/Clause	Protocol	Lane Rate (Gbps)
XFP MSA	XFI	10.3125
IEEE 802.3ba-2010	XLPPI	10.3125
Serial-GMII Specification V1.7	1GE SGMII	1.25
IEEE 802.3ba	XLAUI	10.3125
IEEE 802.3ap 2007	10GBASE-KR	10.3125
IEEE 803.3ap-2007 IEEE 802.3an-2006	1000BASE-KX/CX	1.25
CEI 4.0	CEI-11G SR/MR/LR	9.95 – 11.2
	CEI-6G SR/LR	4.976 – 6.375
PCIe BASE 3.0 PIPE 3.0	PCIe 3.0	8
SMPTE 259M	SDI SD	0.27
SMPTE 292M	SDI HD	1.485/1.483
SMPTE ST 424	SDI 3G	2.97/2.967
SMPTE ST 2081	SDI 6G	5.94/5.934
SMPTE ST 2082	SDI 12G	11.88/11.868
JESD204B	JESD204B	up to 12.5
DP 2.0	DisplayPort 1.4	1.62
		2.7
		5.4
		8.1
	DisplayPort 2.0	10
Serial ATA revision 3.5a T10/BSR INCITS 519	Sata Gen 3	1.5 – 6

continued...

Specification/Clause	Protocol	Lane Rate (Gbps)
	SAS	1.5 – 12.0
HDMI 1.4	HDMI	3.4
HDMI 2.0		6
HDMI 2.1		–
SLVS-EC Specification Version 1.0	SLVS-EC RX	2.376
SLVS-EC Specification Version 2.0		5
SFF-8402	SFP+	9.95 – 11.2
SFF-8431 4.1		
SFF-8431 Rev 4.1		
SFF-8418		
USB 3.1	USB 3.1 Gen 1	5
RapidIO™ Interconnect Specification	SRIO	2 to 12.5(2x6.25)

HPS Performance Specifications

This section provides hard processor system (HPS) specifications and timing.

HPS Clock Performance

Table 63. Maximum HPS Clock Frequencies

For specification status, see the *Data Sheet Status* table

Performance	V_{CCL_HPS} (V)[97]	Cortex-A55 Core Frequency (MHz)	DSU (DynamIQ Shared Unit) Frequency (MHz) (mpu_free_clk)	L3 Frequency (MHz) (l3_main_free_clk)	LPDDR4 Clock (MHz)
–6 speed grade	Fixed: 0.78	800	533	400	Refer to the Memory Standards Supported table.
–7 speed grade	Fixed: 0.75	800	533	400	

(97) V_{CCL_HPS} refers to $V_{CCL\_HPS\_CORE0\_CORE1}$ for HPS Cortex-A55 core 0 and core 1 power rail

Related Information

- HPS Power Supply Operating Conditions on page 20
- Memory Standards Supported on page 58

HPS Internal Oscillator Frequency

Table 64. HPS Internal Oscillator Frequency

For specification status, see the *Data Sheet Status* table

Description	Min	Typ	Max	Unit
Internal oscillator frequency	150	300	400	MHz

HPS PLL Specifications

Table 65. HPS PLL Input Requirements

The main HPS PLL receives its clock signals from the `HPS_OSC_CLK` pin. Refer to the *Pin Connection Guidelines* of this device for information about assigning this pin.

For specification status, see the *Data Sheet Status* table

Description	Min	Typ	Max	Unit
Clock input range	25	—	125	MHz
Clock input accuracy	—	—	50	ppm
Clock input duty cycle	45	50	55	%

Table 66. HPS PLL Performance

For specification status, see the *Data Sheet Status* table

Description	Min	Max	Unit
Main PLL VCO output	—	3,500	MHz
Peripheral PLL VCO output	—	3,500	MHz
h2f_user0_clk(98)	—	500	MHz
h2f_user1_clk(98)	—	500	MHz

HPS Cold Reset

Table 67. HPS Cold Reset

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Max	Unit
t_{RST0}	Minimum time for `HPS_COLD_nRESET` asserted(99)	3	—	ms

HPS SPI Timing Characteristics

Table 68. SPI Master Timing Requirements

You can adjust the input delay timing by programming the `rx_sample_dly` register.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
$T_{spi\_ref\_clk}$	The period of the SPI internal reference clock, sourced from `l4_main_clk`	2.5	—	—	ns
F_{clk}	SPIM_CLK clock frequency	—	—	60	MHz
T_{clk}	SPIM_CLK clock period	16.67	—	—	ns
$T_{dutycycle}$	SPIM_CLK duty cycle	45	50	55	%
T_{ck_jitter}	SPIM_CLK output jitter	—	—	2	%
T_{dio}	Master-out slave-in (MOSI) output skew	–3	—	2	ns
$T_{dssfrst}$ (100)	SPI_SS_N asserted to first SPIM_CLK edge	$(1.5 \times T_{clk}) - 2$	—	—	ns

continued...

(98) The HPS PLL provides this clock to the FPGA fabric.

(99) `HPS_COLD_nRESET` may be ignored if HPS is not running or if the device is being configured.

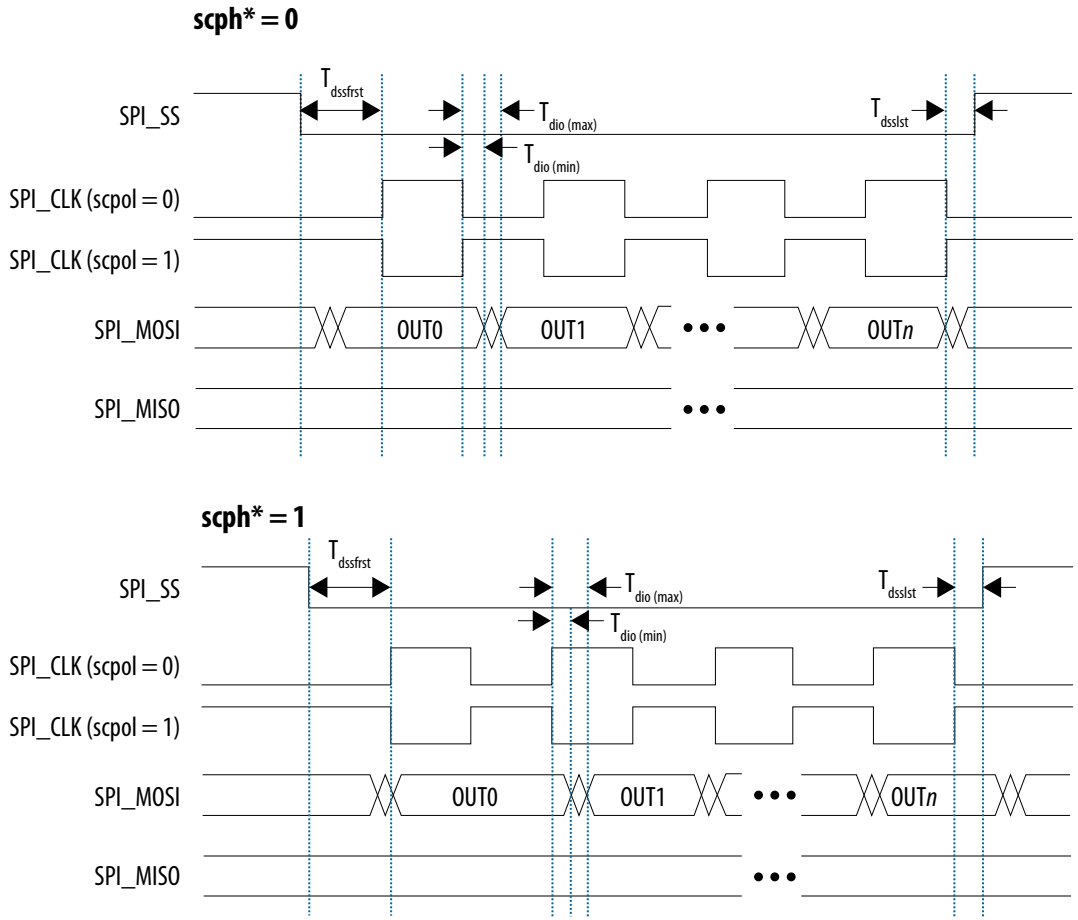
Symbol	Description	Min	Typ	Max	Unit
T_{dsslst} (100)	Last SPIM_CLK edge to SPI_SS_N deasserted	T_{clk} – 2	—	—	ns
T_{su} (101)	SPIM_MISO setup time with respect to SPIM_CLK capture edge	5.0 – (`rx_sample_dly` x $T_{spi\_ref\_clk}$)(102)	—	—	ns
T_h (101)	Input hold in respect to SPIM_CLK capture edge	1.3 + (`rx_sample_dly` x $T_{spi\_ref\_clk}$)(102)	—	—	ns

(100) SPI_SS_N behavior differs depending on Motorola SPI protocols, Texas Instruments Synchronous Serial Protocols, or National Semiconductor Microwire operational mode.

(101) The capture edge differs depending on the operational mode. For Motorola SPI, the capture edge can be the rising or falling edge depending on the `scpol` register bit; for Texas Instruments Synchronous Serial Protocols, the capture edge is the falling edge; for National Semiconductor Microwire, the capture edge is the rising edge.

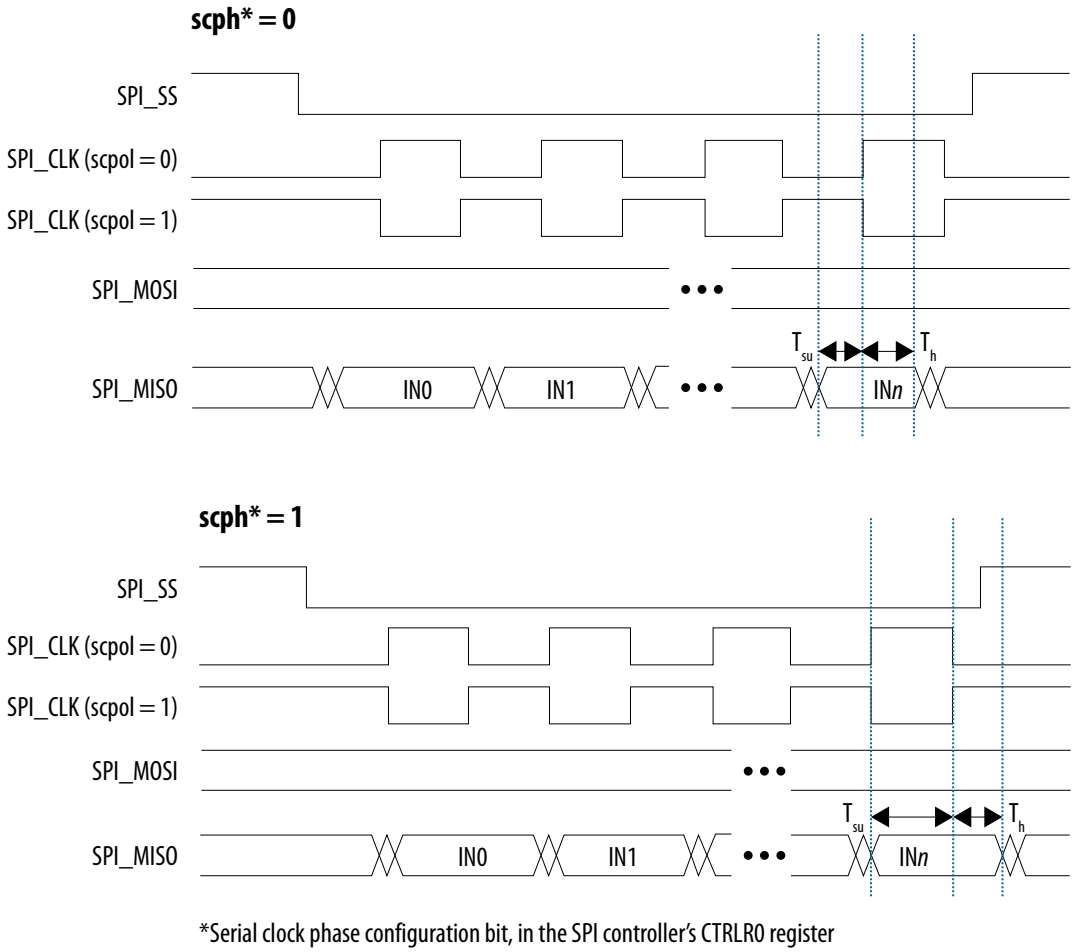
(102) Valid values of `rx_sample_dly` range from 1 to 64 (units are in $T_{spi\_ref\_clk}$ steps).

Figure 3. SPI Master Output Timing Diagram



*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

Figure 4. SPI Master Input Timing Diagram



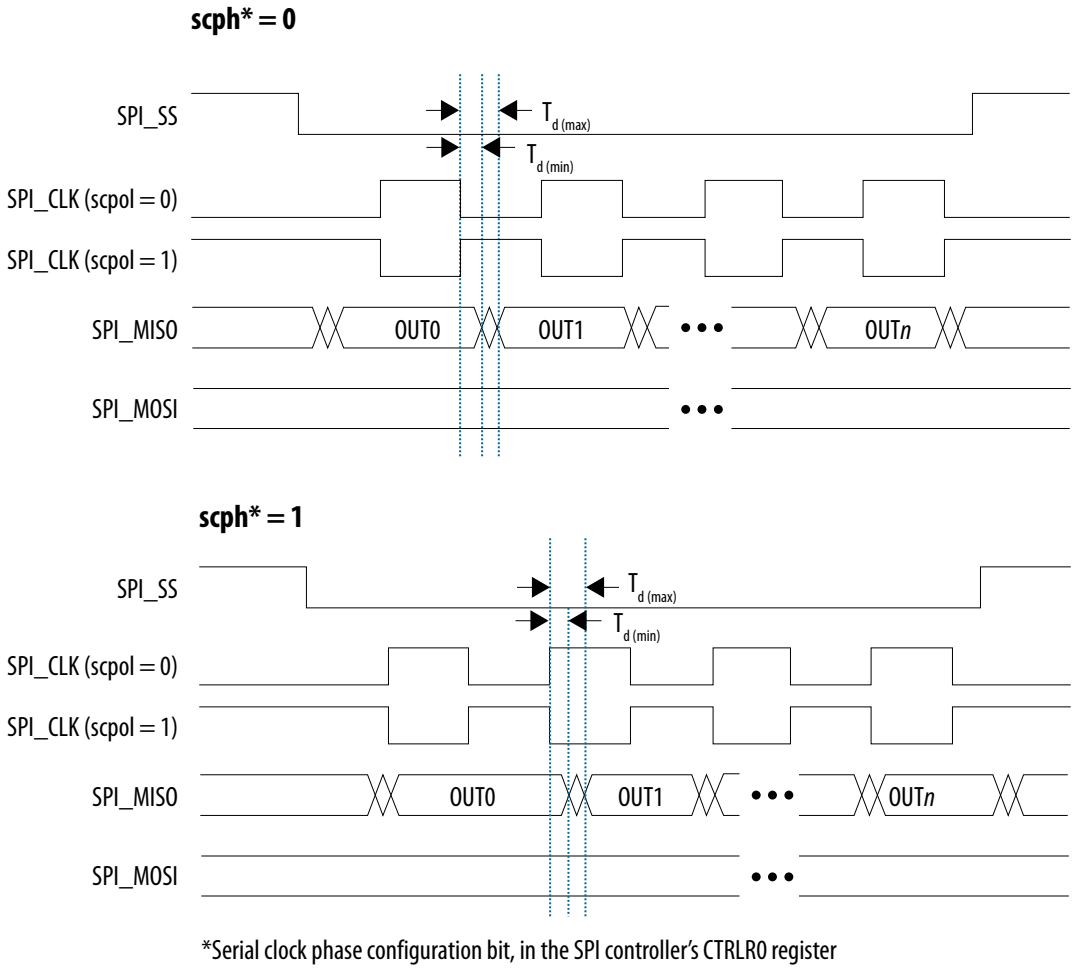
*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

Table 69. SPI Slave Timing Requirements

For specification status, see the *Data Sheet Status* table

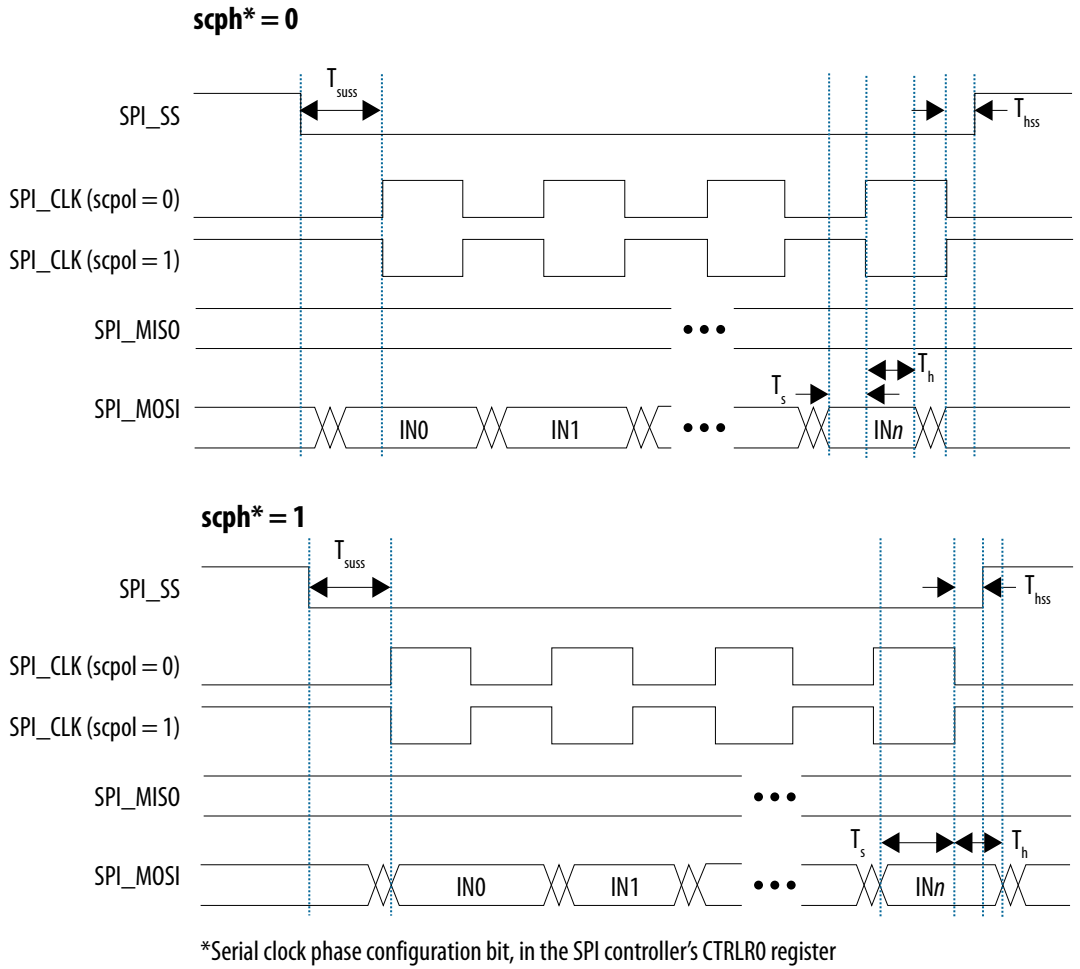
Symbol	Description	Min	Typ	Max	Unit
$T_{spi\_ref\_clk}$	The period of the SPI internal reference clock, sourced from `l4_main_clk`	2.5	—	—	ns
F_{clk}	SPIM_CLK clock frequency	—	—	33	MHz
T_{clk}	SPIM_CLK clock period	30	—	—	ns
$T_{dutycycle}$	SPIM_CLK duty cycle	45	50	55	%
T_d	Master-in slave-out (MISO) output skew	$(2 \times T_{spi\_ref\_clk}) + 3$	—	$(3 \times T_{spi\_ref\_clk}) + 11$	ns
T_{su}	Master-out slave-in (MOSI) setup time	4	—	—	ns
T_h	Master-out slave-in (MOSI) hold time	9	—	—	ns
T_{suss}	SPI_SS_N asserted to first SPIM_CLK edge	$T_{spi\_ref\_clk} + 4.2$	—	—	ns
T_{hss}	Last SPIM_CLK edge to SPI_SS_N deasserted	$T_{spi\_ref\_clk} + 4.2$	—	—	ns

Figure 5. SPI Slave Output Timing Diagram



*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

Figure 6. SPI Slave Input Timing Diagram



*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

HPS SD/eMMC Timing Characteristics

Table 70. HPS Secure Digital (SD)/Embedded MultiMediaCard (eMMC) Timing Requirements

Supports SD devices up to V6.1. Supports SDIO devices up to V4.1. Supports SD/eMMC devices up to V5.1.

These timings apply to SD, MMC, and eMMC cards operating at 1.8 V.

For specification status, see the *Data Sheet Status* table

Symbol	Description		Min	Typ	Max	Unit
T_{sdmmc_cclk}	SD SDMMC_CCLK clock period	Identification mode, 400 kHz	2,500	—	—	ns
		SDR12, 25 MHz	40	—	—	ns
		SDR25, 50 MHz	20	—	—	ns
		SDR50, 100 MHz	10	—	—	ns
		SDR104, <200 MHz	5	—	—	ns
		DDR50, 50 MHz	20	—	—	ns
	eMMC SDMMC_CCLK clock period	Legacy, 25MB/s, 25 MHz	40	—	—	ns
		HS_SDR, 50MB/s, 50 MHz	20	—	—	ns
		HS_DDR, 100MB/s, 50 MHz	20	—	—	ns
		HS200, SDR, 200MB/s, 200 MHz	5	—	—	ns
		HS400, DDR, 400MB/s, 200 MHz	5	—	—	ns
$T_{dutycycle}$	SDMMC_CCLK duty cycle		45	50	55	%
$T_{sdmmc\_cclk\_jitter}$	SDMMC_CCLK output jitter		—	—	2	%
T_{sdmmc_clk}	Internal reference clock before division by 4 (200 MHz)		5	—	—	ns

None of the HPS I/Os supports 3 V mode, while SD/MMC cards must operate at 3 V at power on. eMMC devices can operate at 1.8 V at power on.

Note: SD cards power up at 3 V. To support SD, your design must include a level shifter between the SD card and the HPS SD/MMC interface.

Table 71. SD Input Timing (SDR104, SDR50, SDR25, SDR12)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{is}	SDMMC_CMD/ SDMMC_DATA[7:0] input setup (SDR104)	1.4	—	—	ns
	SDMMC_CMD/ SDMMC_DATA[7:0] input setup (SDR50)	3	—	—	ns
	SDMMC_CMD/ SDMMC_DATA[7:0] input setup (SDR25)	6	—	—	ns
	SDMMC_CMD/ SDMMC_DATA[7:0] input setup (SDR12)	5	—	—	ns
T_{ih}	SDMMC_CMD/ SDMMC_DATA[7:0] input hold (SDR104)	0.8	—	—	ns
	SDMMC_CMD/ SDMMC_DATA[7:0] input hold (SDR50)	0.8	—	—	ns
	SDMMC_CMD/ SDMMC_DATA[7:0] input hold (SDR25)	2	—	—	ns
	SDMMC_CMD/ SDMMC_DATA[7:0] input hold (SDR12)	5	—	—	ns

Figure 7. SD Input (SDR104, SDR50, SDR25, SDR12) Timing Diagram

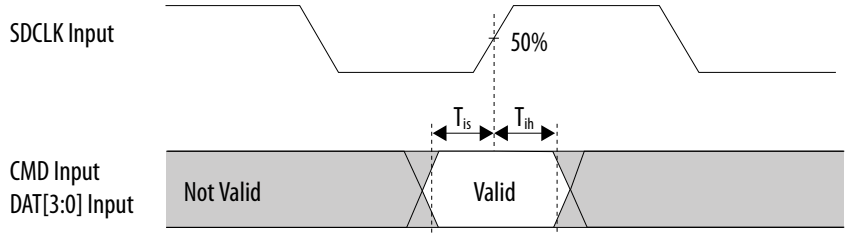


Table 72. SD Output Timing (SDR50, SDR25, SDR12)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{odly}	SDMMC_CMD/ SDMMC_DATA[7:0] output delay (SDR50)	—	—	7.5	ns
	SDMMC_CMD/ SDMMC_DATA[7:0] output delay (SDR25, SDR12)	—	—	14	ns
T_{ohld}	SDMMC_CMD/ SDMMC_DATA[7:0] output hold	1.5	—	—	ns

Figure 8. SD Output (SDR50, SDR25, SDR12) Timing Diagram

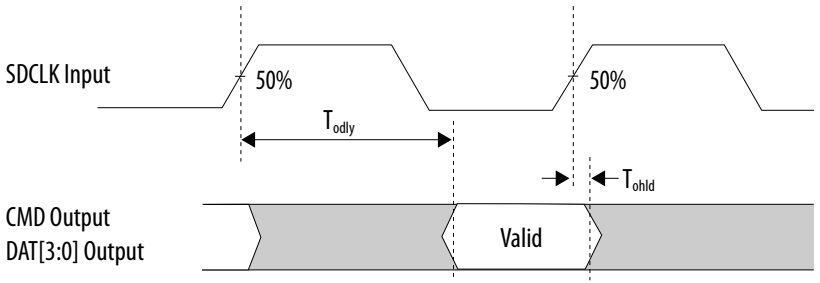


Table 73. SD Output Timing (SDR104)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{op}	SDMMC_CMD/ SDMMC_DATA[7:0] output phase	0	—	10	ns
ΔT_{op}	SDMMC_CMD/ SDMMC_DATA[7:0] output delay variation due to temperature change after tuning	–350	—	1,550	ps
T_{odw}	SDMMC_CMD/ SDMMC_DATA[7:0] output hold	3	—	—	ns

Figure 9. SD Output (SDR104) Timing Diagram

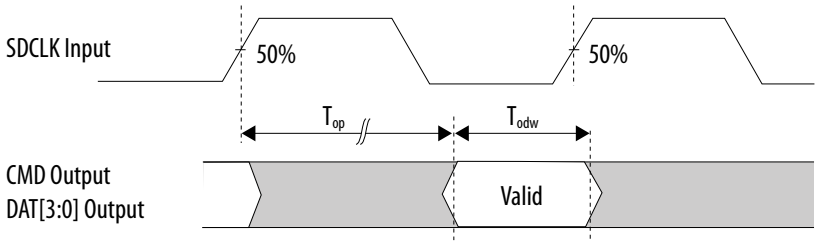


Table 74. SD Timing (DDR50)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{isu}	SDMMC_CMD input setup	6	—	—	ns
T_{ih}	SDMMC_CMD input hold	0.8	—	—	ns
T_{odly}	SDMMC_CMD output delay	—	—	13.7	ns
T_{oh}	SDMMC_CMD output hold	1.5	—	—	ns

continued...

Symbol	Description	Min	Typ	Max	Unit
T_{isu2x}	SDMMC_DATA[7:0] input setup	3	—	—	ns
T_{ih2x}	SDMMC_DATA[7:0] input hold	0.8	—	—	ns
T_{odly2x}	SDMMC_DATA[7:0] output delay	—	—	7	ns
T_{odly2x}	SDMMC_DATA[7:0] output hold	1.5	—	—	ns

Figure 10. SD (DDR50) Timing Diagram

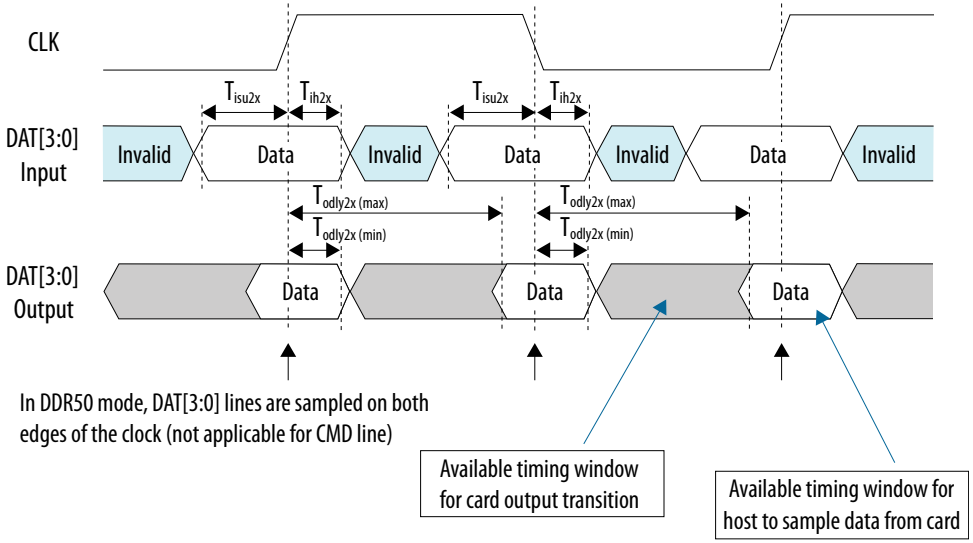
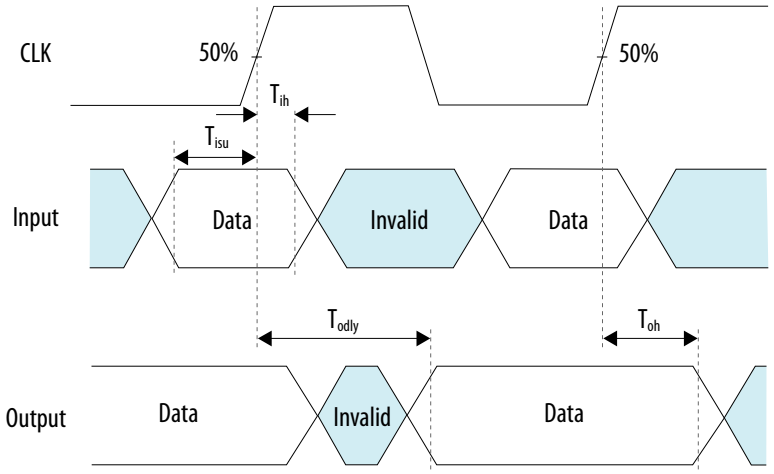


Table 75. eMMC Timing (Legacy, HS_SDR)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{isu}	EMMC_CMD_DATA input setup (Legacy)	3	—	—	ns
	EMMC_CMD_DATA input setup (HS_SDR)	3	—	—	ns
T_{ih}	EMMC_CMD DATA_input hold (Legacy)	3	—	—	ns
	EMMC_CMD DATA_input hold (HS_SDR)	3	—	—	ns
T_{odly}	EMMC_CMD_DATA output delay (Legacy)	—	—	13.7	ns
	EMMC_CMD_DATA output delay (HS_SDR)	—	—	13.7	ns
T_{oh}	EMMC_CMD_DATA output hold (Legacy)	8.3	—	—	ns
	EMMC_CMD DATA_output hold (HS_SDR)	2.5	—	—	ns

Figure 11. eMMC (Legacy, HS_SDR) Timing Diagram



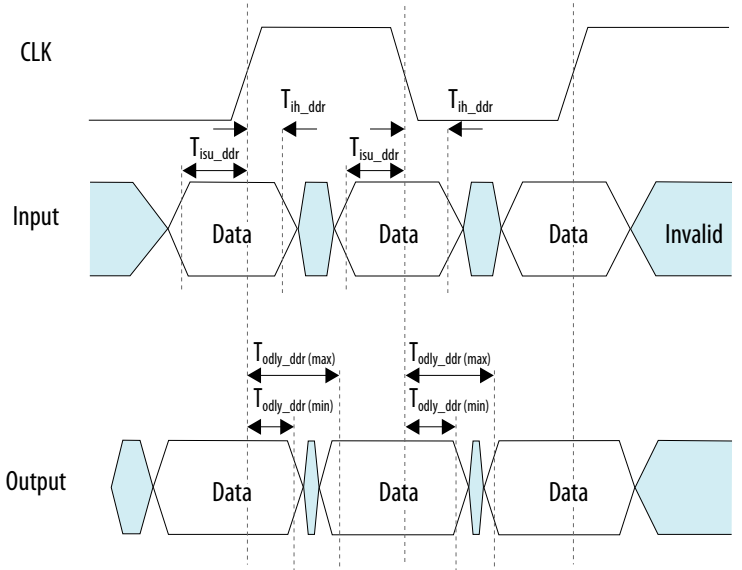
Data must always be sampled on the rising edge of the clock.

Table 76. eMMC Timing (HS_DDR)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{isu_ddr}	EMMC_CMD_DATA input setup	2.5	—	—	ns
T_{ih_ddr}	EMMC_CMD DATA_input hold	2.5	—	—	ns
T_{odly_ddr}	EMMC_CMD_DATA output delay (max=delay, min=hold)	1.5	—	7	ns

Figure 12. eMMC (HS_DDR) Timing Diagram



In DDR mode data on DAT[7:0] lines are sampled on both edges of the clock (not applicable for CMD line)

Table 77. eMMC Timing (HS200)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{isu}	EMMC_CMD_DATA input setup	1.4	—	—	ns
T_{ih}	EMMC_CMD DATA_input hold	0.8	—	—	ns

continued...

Symbol	Description	Min	Typ	Max	Unit
T_{ph}	SDMMC_CMD/ SDMMC_DATA[7:0] output phase	0	—	10	ns
ΔT_{ph}	SDMMC_CMD/ SDMMC_DATA[7:0] output delay variation due to temperature change after tuning	–350	—	1,550	ps
T_{vw}	SDMMC_CMD/ SDMMC_DATA[7:0] output hold	3	—	—	ns

Figure 13. eMMC Input (HS200) Timing Diagram

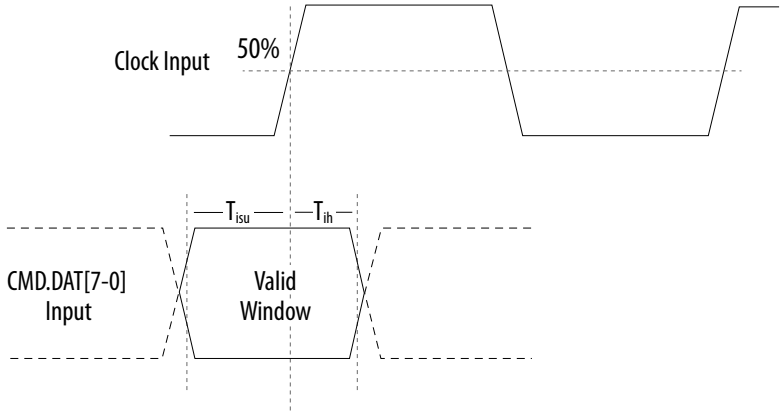


Figure 14. eMMC Output (HS200) Timing Diagram

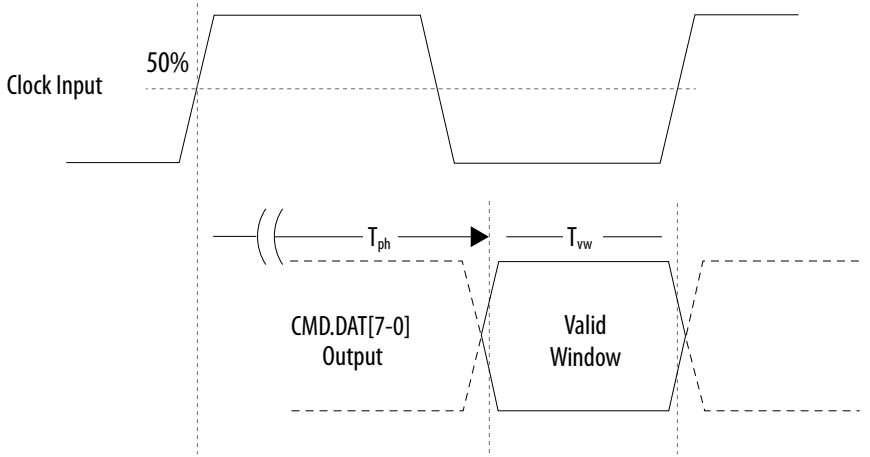


Table 78. eMMC Timing (HS400)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{isu_ddr}	EMMC_CMD_DATA input setup	0.4	—	—	ns
T_{ih_ddr}	EMMC_CMD DATA_input hold	0.4	—	—	ns
T_{rq}	SDMMC_CMD/ SDMMC_DATA[7:0] output phase	0	—	10	ns
ΔT_{rq}	SDMMC_CMD/ SDMMC_DATA[7:0] output delay variation due to temperature change after tuning	–350	—	200	ps
T_{rqh}	SDMMC_CMD/ SDMMC_DATA[7:0] output hold	2	—	—	ns

Figure 15. eMMC Input (HS400) Timing Diagram

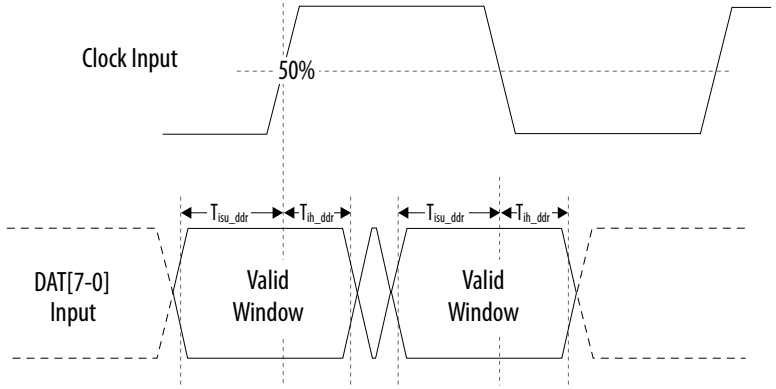
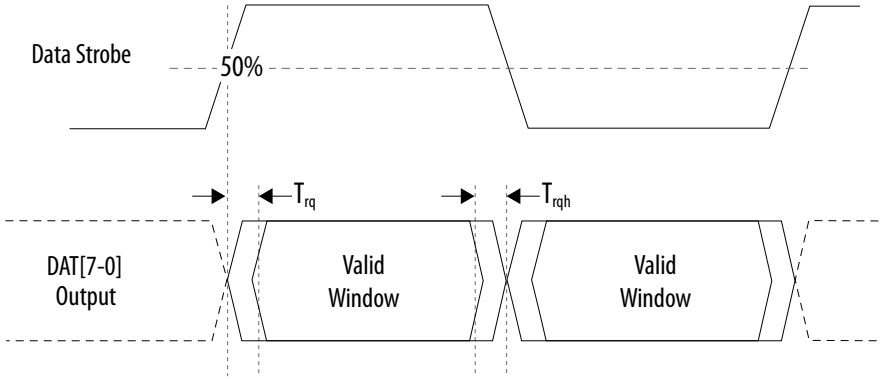


Figure 16. eMMC Output (HS400) Timing Diagram



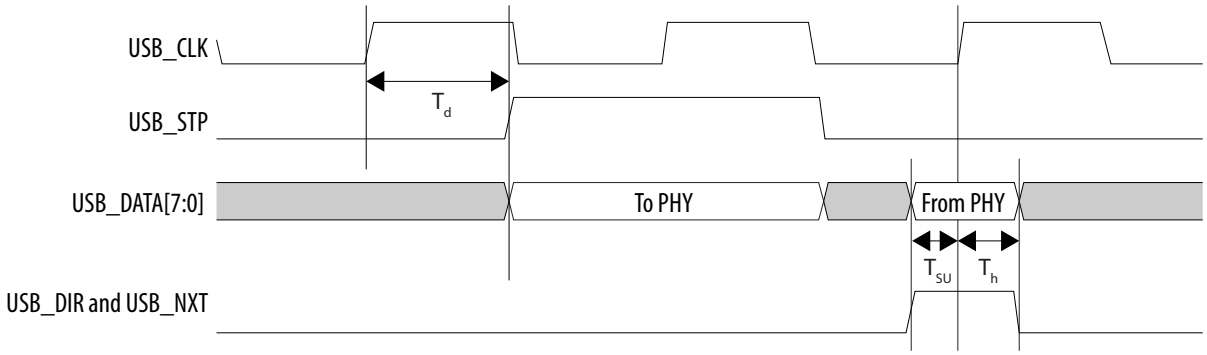
HPS USB 2.0 Timing Characteristics

Table 79. HPS USB 2.0 Transceiver Macrocell Interface Plus (UTMI+) Low Pin Interface (ULPI) Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
F_{usb_clk}	USB_CLK clock frequency	—	60	—	MHz
T_{usb_clk}	USB_CLK clock period	—	16.667	—	ns
T_d	Clock to USB_STP/ USB_DATA[7:0] output delay	2	—	7	ns
T_{su}	Setup time for USB_DIR/ USB_NXT/USB_DATA[7:0]	4	—	—	ns
T_h	Hold time for USB_DIR/ USB_NXT/USB_DATA[7:0]	1	—	—	ns

Figure 17. USB ULPI Timing Diagram



Note: The USB interface supports single data rate (SDR) timing only.

Note: If you need to adjust the timings of certain signals, you can use the HPS registers `Pin_Mux.io0_delay` through `Pin_Mux.io47_delay` to allow software to set the delay chains in each of the dedicated I/Os. For example, to add output and input delay to the USB_DATA3 signal (HPS_IOA_8), program Pin_Mux.io7_delay.output_val_en = 1, and Pin_Mux.io7_delay.output_val = 15 to add approximately 1.4 ns output delay from the HPS, and program Pin_Mux.io7_delay.input_val_en = 3, and Pin_Mux.io7_delay.input_val = 30 to add approximately 2.8 ns input delay into the HPS. See HPS Programmable I/O Timing Characteristics for more information.

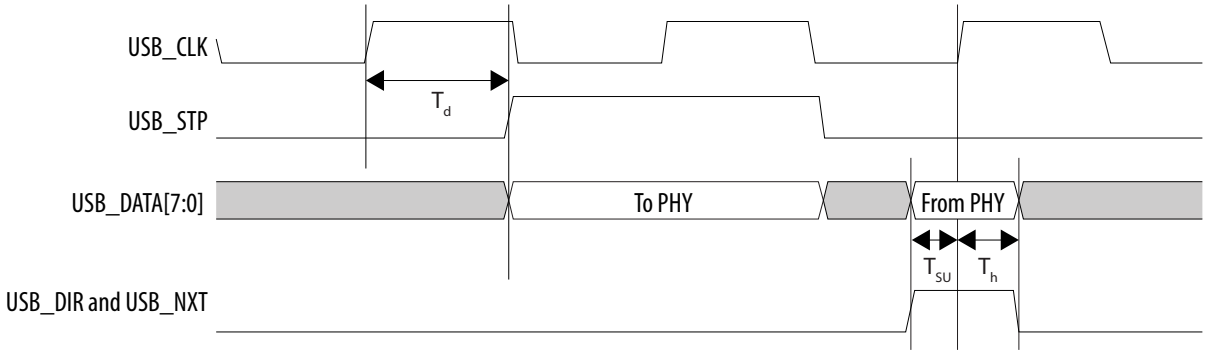
HPS USB 3.1 Timing Characteristics

Table 80. HPS USB 3.1 Transceiver Macrocell Interface Plus (UTMI+) Low Pin Interface (ULPI) Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
F_{usb_clk}	USB_CLK clock frequency	—	60	—	MHz
T_{usb_clk}	USB_CLK clock period	—	16.667	—	ns
T_d	Clock to USB_STP/ USB_DATA[7:0] output delay	2	—	7	ns
T_{su}	Setup time for USB_DIR/ USB_NXT/USB_DATA[7:0]	4	—	—	ns
T_h	Hold time for USB_DIR/ USB_NXT/USB_DATA[7:0]	1	—	—	ns

Figure 18. USB ULPI Timing Diagram



Note: The USB interface supports single data rate (SDR) timing only.

Note: If you need to adjust the timings of certain signals, you can use the HPS registers `Pin_Mux.io0_delay` through `Pin_Mux.io47_delay` to allow software to set the delay chains in each of the dedicated I/Os. For example, to add output and input delay to the USB_DATA3 signal (HPS_IOA_8), program Pin_Mux.io7_delay.output_val_en = 1, and Pin_Mux.io7_delay.output_val = 15 to add approximately 1.4 ns output delay from the HPS, and program Pin_Mux.io7_delay.input_val_en = 3, and Pin_Mux.io7_delay.input_val = 30 to add approximately 2.8 ns input delay into the HPS. See HPS Programmable I/O Timing Characteristics for more information.

HPS Ethernet Media Access Controller (EMAC) Timing Characteristics

Table 81. Reduced Gigabit Media Independent Interface (RGMII) TX Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (1000Base-T)	TX_CLK clock period (125 MHz)	—	8	—	ns
T_{clk} (100Base-T)	TX_CLK clock period (25 MHz)	—	40	—	ns
T_{clk} (10Base-T)	TX_CLK clock period (2.5 MHz)	—	400	—	ns
$T_{dutycycle}$ (1000Base-T)	TX_CLK duty cycle	45	50	55	%
$T_{dutycycle}$ (10/100Base-T)	TX_CLK duty cycle	40	50	60	%
T_d (103) (104)	TXD/TX_CTL to TX_CLK output skew	–0.5	—	0.5	ns

(103) Rise and fall times depend on the I/O standard, drive strength, and loading. Altera recommends simulating your configuration.

(104) If you connect a PHY that does not implement clock-to-data skew, you can delay TX_CLK by 1.5–2.0 ns with the HPS I/O programmable delay, to meet the PHY's 1 ns data-to-clock skew requirement.

Figure 19. RGMII TX Timing Diagram

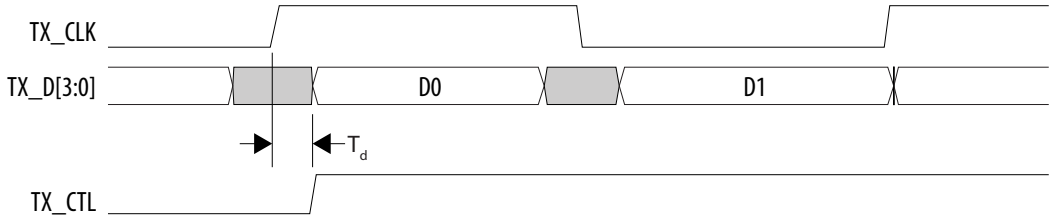


Table 82. RGMII RX Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (1000Base-T)	RX_CLK clock period (125 MHz)	—	8	—	ns
T_{clk} (100Base-T)	RX_CLK clock period (25 MHz)	—	40	—	ns
T_{clk} (10Base-T)	RX_CLK clock period (2.5 MHz)	—	400	—	ns
$T_{dutycycle}$ (1000Base-T)	RX_CLK duty cycle	45	50	55	%
$T_{dutycycle}$ (10/100Base-T)	RX_CLK duty cycle	40	50	60	%
T_{su}	RX_D/RX_CTL to RX_CLK setup time	1	—	—	ns
T_h (105)	RX_CLK to RX_D/RX_CTL hold time	1	—	—	ns

(105) If you connect a PHY that does not implement clock-to-data skew, you can meet the HPS EMAC's 1 ns setup time by delaying RX_CLK by 1.5–2 ns, using the HPS I/O programmable delay.

Figure 20. RGMII RX Timing Diagram

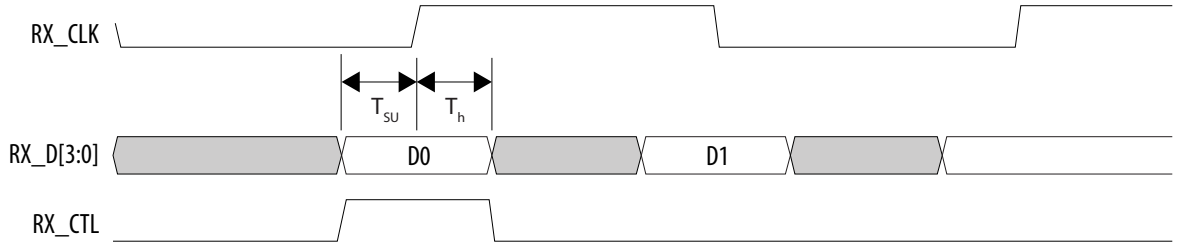
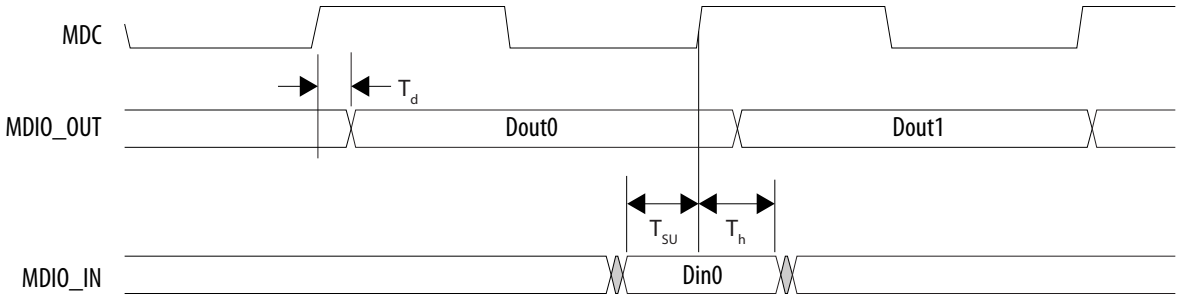


Table 83. Management Data Input/Output (MDIO) Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
F_{clk}	MDC clock frequency	—	—	2.5	MHz
T_{clk}	MDC clock period	400	—	—	ns
T_d	MDC to MDIO output data delay	10	—	300	ns
T_{su}	Setup time for MDIO data	10	—	—	ns
T_h	Hold time for MDIO data	0	—	—	ns

Figure 21. MDIO Timing Diagram



SGMII Timing Requirements

SGMII operating mode is supported through FPGA fabric using SGMII PCS soft IP and LVDS SERDES IP. Refer to the *LVDS SERDES Specifications* section for timing specifications.

SGMII+ operating mode is supported through FPGA fabric using SGMII+ PCS soft IP and serial transceiver interface. Refer to the *Transceiver Performance Specifications* section for timing specifications.

Related Information

- LVDS SERDES Specifications on page 53
- GTS Transceiver Performance Specifications on page 60

HPS I²C Timing Characteristics

Table 84. HPS I²C Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
F_{clk}	Serial clock (SCL) clock frequency	—	100	—	400	KHz
T_{clk}	Serial clock (SCL) clock period	10	—	2.5	—	µs
T_{clk_jitter}	I²C clock output jitter	—	2	—	2	%
T_{HIGH} (106)	SCL high period	4(107)	—	0.6(108)	—	µs

continued...

(106) You can adjust T_{HIGH} using the `ic_ss_scl_hcnt` or `ic_fs_scl_hcnt` register.

(107) The recommended minimum setting for `ic_ss_scl_hcnt` is 428. Refer to the SCL_High_time equation in the *Hard Processor System Technical Reference Manual*.

(108) The recommended minimum setting for `ic_fs_scl_hcnt` is 75. Refer to the SCL_High_time equation in the *Hard Processor System Technical Reference Manual*.

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
T_{LOW} (109)	SCL low period	4.7(110)	—	1.3(111)	—	µs
T_{SU_DAT}	Setup time for serial data line (SDA) data to SCL	0.25	—	0.1	—	µs
T_{HD_DAT} (112)	Hold time for SCL to SDA data	0	3.15	0	0.6	µs
T_{VD_DAT} and T_{VD_ACK} (113)	SCL to SDA output data delay	—	3.45(114)	—	0.9(115)	µs
T_{SU_STA}	Setup time for a repeated start condition	4.7	—	0.6	—	µs
T_{HD_STA}	Hold time for a repeated start condition	4	—	0.6	—	µs
T_{SU_STO}	Setup time for a stop condition	4	—	0.6	—	µs

continued...

(109) You can adjust T_{LOW} using the `ic_ss_scl_lcnt` or `ic_fs_scl_lcnt` register.

(110) The recommended minimum setting for `ic_ss_scl_lcnt` is 464. Refer to the SCL_Low_time equation in the *Hard Processor System Technical Reference Manual*.

(111) The recommended minimum setting for `ic_fs_scl_lcnt` is 163. Refer to the SCL_Low_time equation in the *Hard Processor System Technical Reference Manual*.

(112) T_{HD_DAT} is affected by the rise and fall time.

(113) T_{VD_DAT} and T_{VD_ACK} are affected by the rise and fall time, as well as the SDA hold time (set by adjusting the `ic_sda_hold` register).

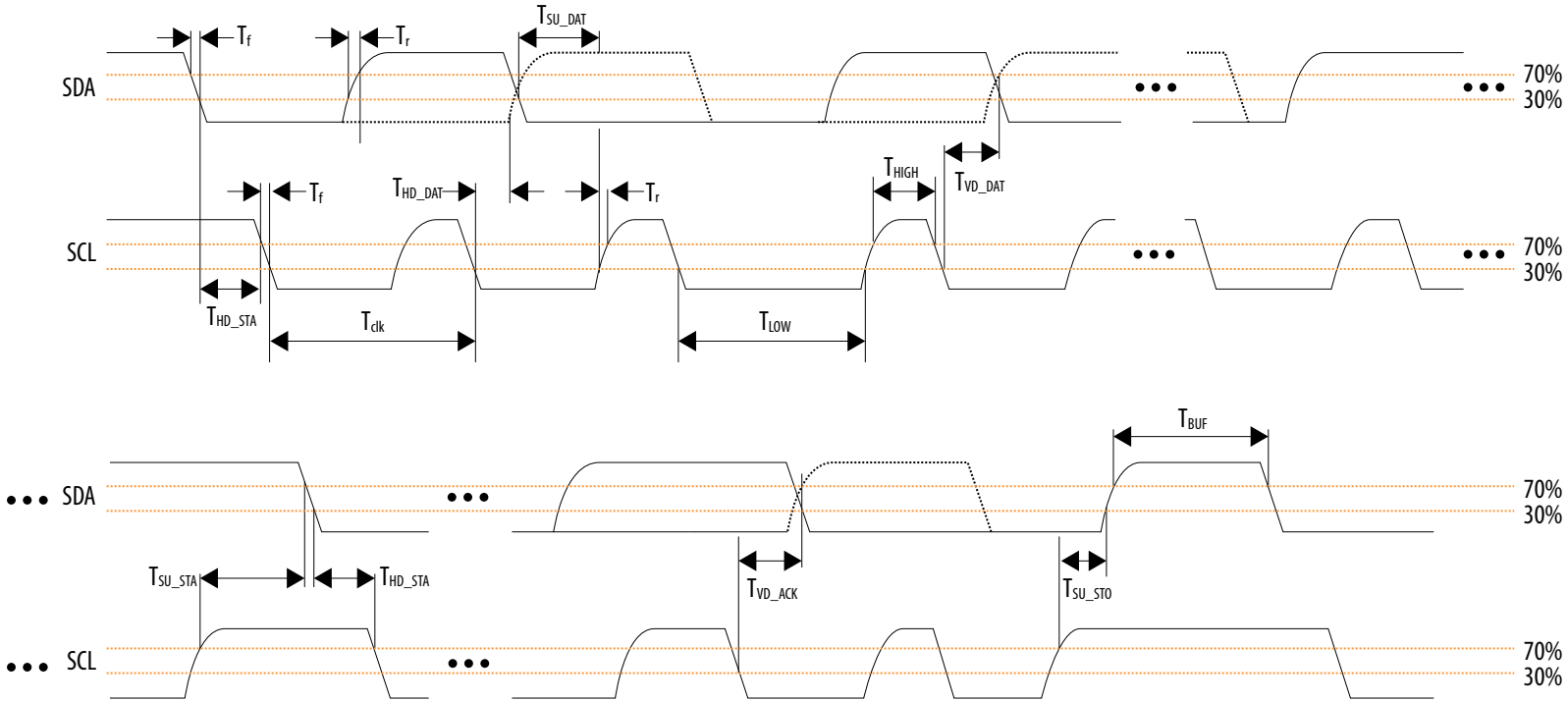
(114) Use maximum `SDA_HOLD` = 240 to be within the specification.

(115) Use maximum `SDA_HOLD` = 60 to be within the specification.

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
T_{BUF}	SDA high pulse duration between STOP and START	4.7	—	1.3	—	µs
T_{scl_r} (116)	SCL rise time	—	1,000	20	300	ns
T_{scl_f} (116)	SCL fall time	—	300	6.54	300	ns
T_{sda_r} (116)	SDA rise time	—	1,000	20	300	ns
T_{sda_f} (116)	SDA fall time	—	300	6.54	300	ns

(116) Rise and fall time parameters vary depending on external factors such as the characteristics of the I/O driver, pull-up resistor value, and total capacitance on the transmission line.

Figure 22. I²C Timing Diagram



HPS I3C Timing Characteristics

Table 85. HPS I3C Timing Requirements When Communicating With I2C Legacy Devices

For specification status, see the *Data Sheet Status* table

Symbol	Description	Fast Mode		Fast Mode Plus		Unit
		Min	Max	Min	Max	
f_{SCL}	Serial clock (SCL) clock frequency	0	0.4	0	1	MHz
T_{SCL}	SCL clock period	2.5	—	1	—	µs
T_{clk_jitter}	I3C clock output jitter	—	2	—	2	%
T_{HIGH}	SCL high period	600	—	260	—	ns
T_{DIG_H}		$T_{HIGH} + T_{scl\_r}$	—	$T_{HIGH} + T_{scl\_r}$	—	ns
T_{LOW}	SCL low period	1,300	—	500	—	ns
T_{DIG_L}		$T_{LOW} + T_{scl\_r}$	—	$T_{LOW} + T_{scl\_r}$	—	ns
T_{SU_DAT}	Setup time for serial data line (SDA) data to SCL	100	—	50	—	ns
T_{HD_DAT}	Hold time for SCL to SDA data	—	—	—	—	—
T_{SU_STA}	Setup time for a repeated start condition	600	—	260	—	ns
T_{HD_STA}	Hold time for a repeated start condition	600	—	260	—	ns
T_{SU_STO}	Setup time for a stop condition	600	—	260	—	ns
T_{BUF}	SDA high pulse duration between STOP and START	1.3	—	0.5	—	µs
T_{scl_r}	SCL rise time	20	300	—	120	ns

continued...

Symbol	Description	Fast Mode		Fast Mode Plus		Unit
		Min	Max	Min	Max	
T_{scl_f}	SCL fall time	20 × (V_{CCIO_HPS} / 5.5 V)(117)	300	20 × (V_{CCIO_HPS} / 5.5 V)(117)	120	ns
T_{sda_r}	SDA rise time	20	300	—	120	ns
T_{sda_f}	SDA fall time	20 × (V_{CCIO_HPS} / 5.5 V)(117)	300	20 × (V_{CCIO_HPS} / 5.5 V)(117)	120	ns
T_{SPIKE}	Pulse width of spikes that the spike filter must suppress	0	50	0	50	ns

Table 86. HPS I3C Open Drain Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Max	Unit
T_{HIGH}	SCL high period	—	41	ns
T_{DIG_H}		—	T_{HIGH} + T_{CF}	ns
T_{HIGH_INIT} (118)	SCL high period (for First Broadcast Address)	200	—	ns
T_{LOW_OD}	SCL low period	200	—	ns
$T_{LOW\_OD\_L}$		T_{LOW_ODmin} + T_{fDA_ODmin}	—	ns
T_{fDA_OD}	SDA signal fall time	T_{CF}	12	ns
T_{SU_OD}	Setup time for serial data line (SDA) data to SCL	3	—	ns
T_{CAS} (118)	Clock after START Condition	38.4 ns	For ENTAS0: 1 µs	—
			For ENTAS1: 100 µs	—

continued...

(117) Refer to the *HPS Power Supply Operating Conditions* section for V_{CCIO_HPS} values.

(118) The controller uses this timing to send the first Broadcast Address after bus initialization, in order to disable the I^2C spike filter for applicable I^3C target devices.

Symbol	Description	Min	Max	Unit
			For ENTAS2: 2 ms	—
			For ENTAS3: 50 ms	—
T_{CBP}	Clock before STOP Condition	$T_{CASmin}/2$	—	s
$T_{MMOverlap}$	Current master to secondary master overlap time during handoff	$T_{DIG\_OD\_Lmin}$	—	ns
T_{AVAL}	Bus available condition	1	—	µs
T_{IDLE}	Bus IDLE condition	200	—	µs
T_{MMLock}	Time internal where new master not driving SDA Low	$T_{AVALmin}$	—	µs

Table 87. HPS I3C Push-Pull Timing Requirements for SDR Mode

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
f_{SCL}	Serial clock (SCL) clock frequency	0.01	12.5	12.9	MHz
T_{CLK}	SCL clock period	77.5 ns	80 ns	100 µs	—
T_{HIGH}	SCL clock high period	24	—	—	ns
T_{DIG_H}		32	—	—	ns
T_{LOW}	SCL clock low period	24	—	—	ns
T_{DIG_L}		32	—	—	ns
T_{HIGH_MIXED}	SCL clock high period for mixed bus(119)	24	—	—	ns
$T_{DIG\_H\_MIXED}$		32	—	45	ns
T_{SCO}	Clock in to data out for slave	—	—	12	ns

continued...

(119) During I3C communication on a mixed bus, to avoid I2C controllers from interpreting I3C signaling as valid I2C signaling, the T_{DIG_H} period must be constrained.

Symbol	Description	Min	Typ	Max	Unit
T_{CR}	SCL rise time	—	—	150e6 × 1/f_{SCL} (capped at 60 ns)	ns
T_{CF}	SCL fall time	—	—	150e6 × 1/f_{SCL} (capped at 60 ns)	ns
T_{HD_PP}	Hold time for SCL to SDA data (master)	T_{CR} + 3 and T_{CF} + 3	—	—	ns
	Hold time for SCL to SDA data (slave)	0	—	—	ns
T_{SU_PP}	SDA signal data setup time	3	—	—	ns
T_{CASr}	Clock after repeated START (Sr)	T_{CASmin}	—	—	ns
T_{CBSr}	Clock before repeated START (Sr)	T_{CASmin} / 2	—	—	ns
C_b	Capacitive load per bus Line (SDA/SCL)	—	—	50	pF

Figure 23. I³C Legacy Mode Timing Diagram

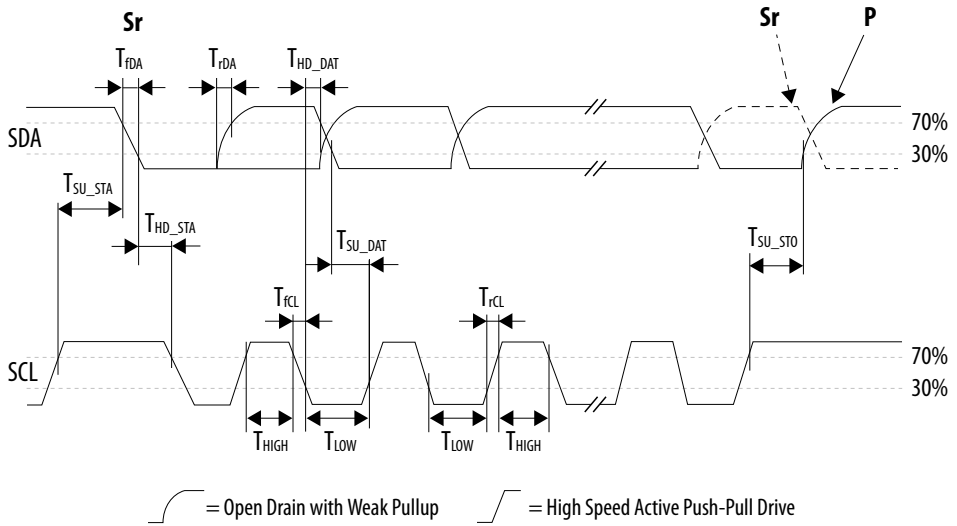


Figure 24. T_{DIG_H} and T_{DIG_L}

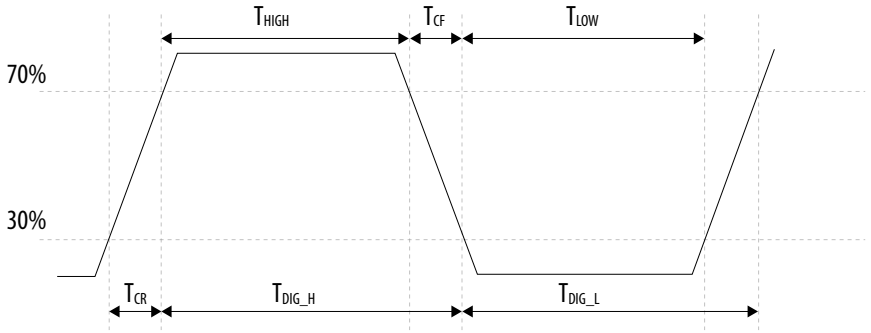


Figure 25. I3C Start Condition Timing Diagram

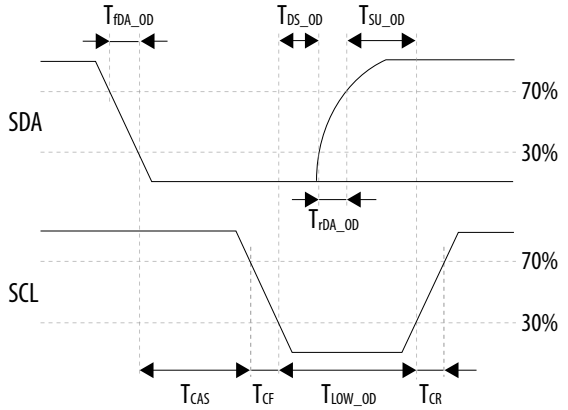


Figure 26. I3C Stop Condition Timing Diagram

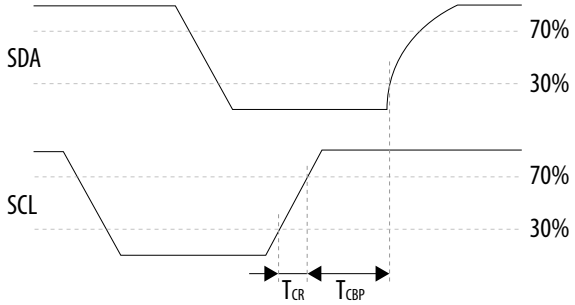


Figure 27. I³C Start Master Out Timing Diagram

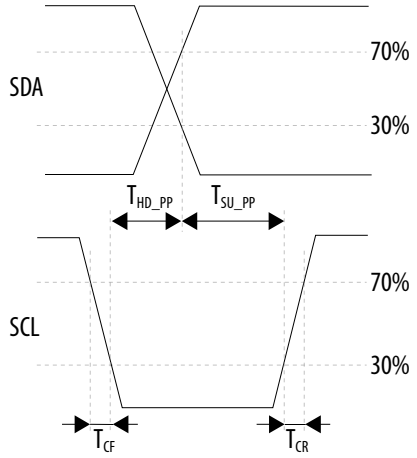


Figure 28. I³C Slave Out Timing Diagram

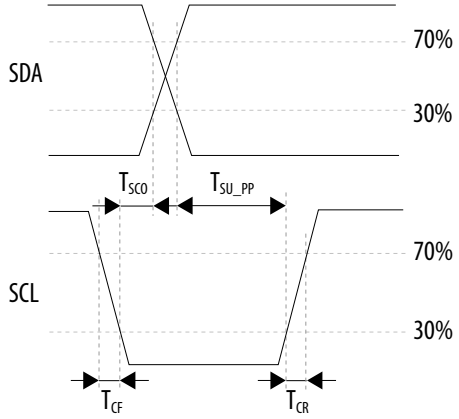
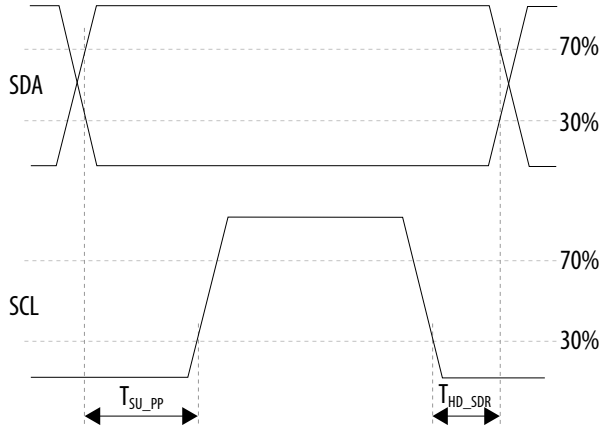


Figure 29. Master SDR Timing Diagram



Related Information

HPS Power Supply Operating Conditions on page 20

HPS NAND Timing Characteristics

Table 88. HPS NAND SDR Timing Requirements

Compatible with the ONFI 1.x and 2.x specifications. Compatible with the Toggle 1.x and 2.x specifications. HPS I/O supports SDR, NV-DDR protocols up to 200 MT/s.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Max	Unit
T_{WP} (120)	Write enable pulse width	10	—	ns
T_{WH} (120)	Write enable hold time	7	—	ns

continued...

(120) This timing is software programmable. Refer to the *NAND Flash Controller* chapter in the *Hard Processor System Technical Reference Manual* for more information about software-programmable timing in the NAND flash controller.

Symbol	Description	Min	Max	Unit
T_{RP} (120)	Read enable pulse width	10	—	ns
T_{REH} (120)	Read enable hold time	7	—	ns
T_{CLS} (120)	Command latch enable to write enable setup time	10	—	ns
T_{CLH} (120)	Command latch enable to write enable hold time	5	—	ns
T_{CS} (120)	Chip enable to write enable setup time	15	—	ns
T_{CH} (120)	Chip enable to write enable hold time	5	—	ns
T_{ALS} (120)	Address latch enable to write enable setup time	10	—	ns
T_{ALH} (120)	Address latch enable to write enable hold time	5	—	ns
T_{DS} (120)	Data to write enable setup time	7	—	ns
T_{DH} (120)	Data to write enable hold time	5	—	ns
T_{WB} (120)	Write enable high to R/B low	—	200	ns
T_{CEA}	Chip enable to data access time	—	100	ns
T_{REA}	Read enable to data access time	—	40	ns
T_{RHZ}	Read enable to data high impedance	—	200	ns
T_{RR}	Ready to read enable low	20	—	ns

Figure 30. NAND SDR Command Latch Timing Diagram

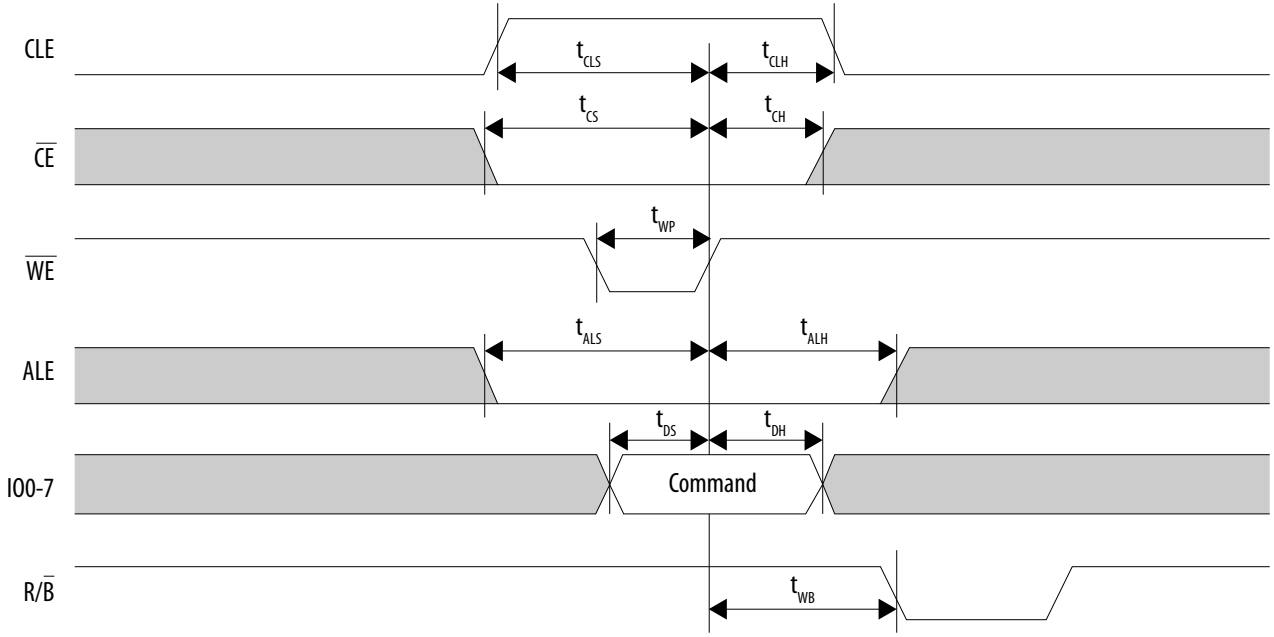


Figure 31. NAND SDR Address Latch Timing Diagram

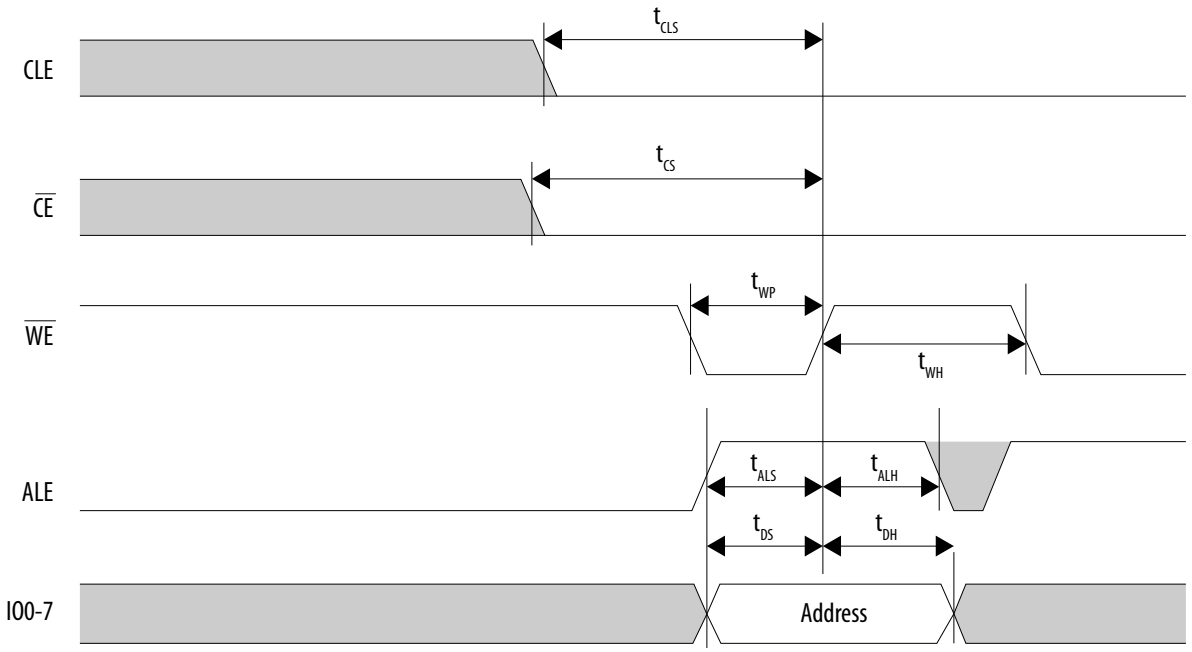


Figure 32. NAND SDR Data Output Cycle Timing Diagram

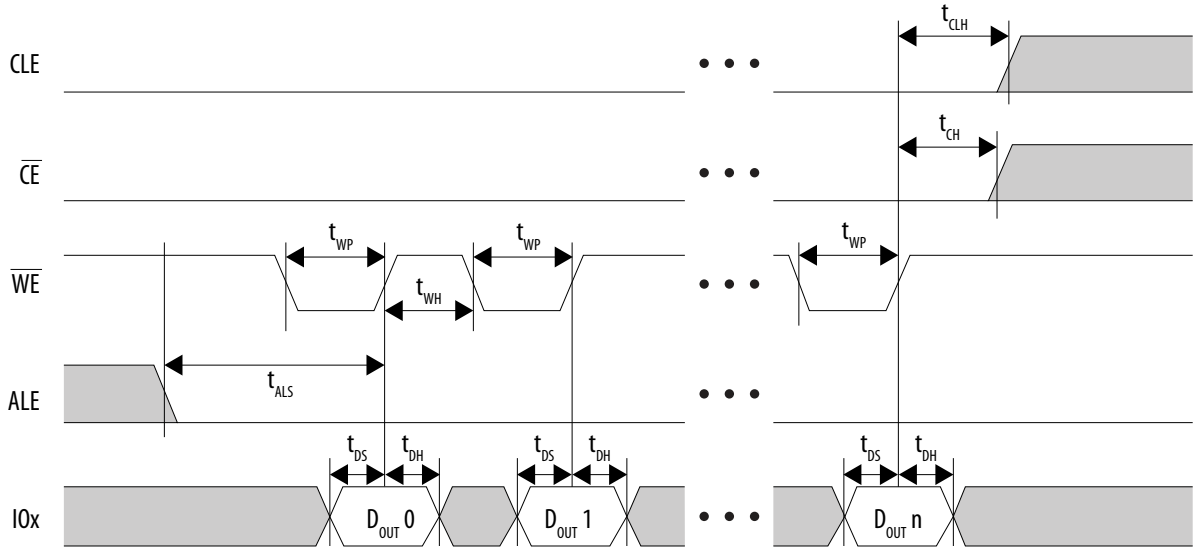


Figure 33. NAND SDR Data Input Cycle Timing Diagram

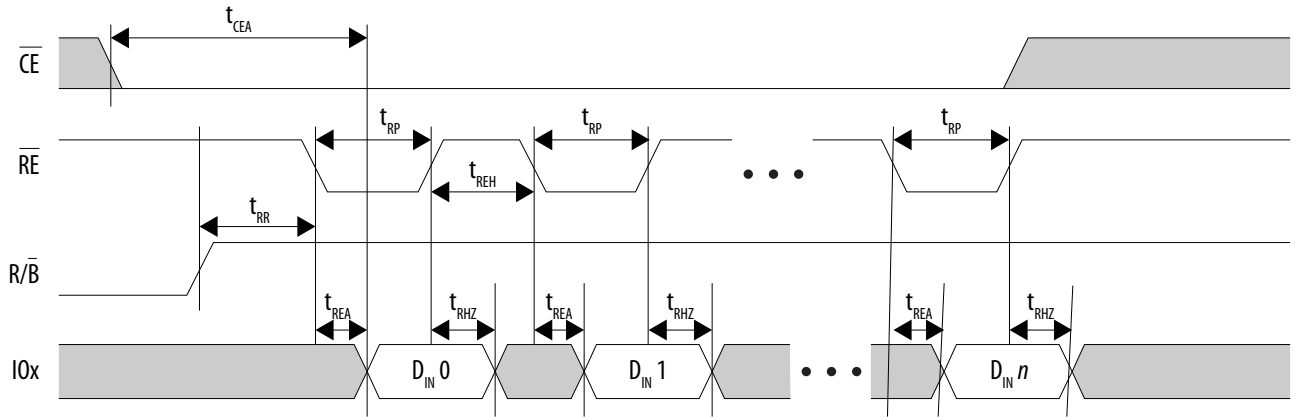


Figure 34. NAND SDR Data Input Timing Diagram for Extended Data Output (EDO) Cycle

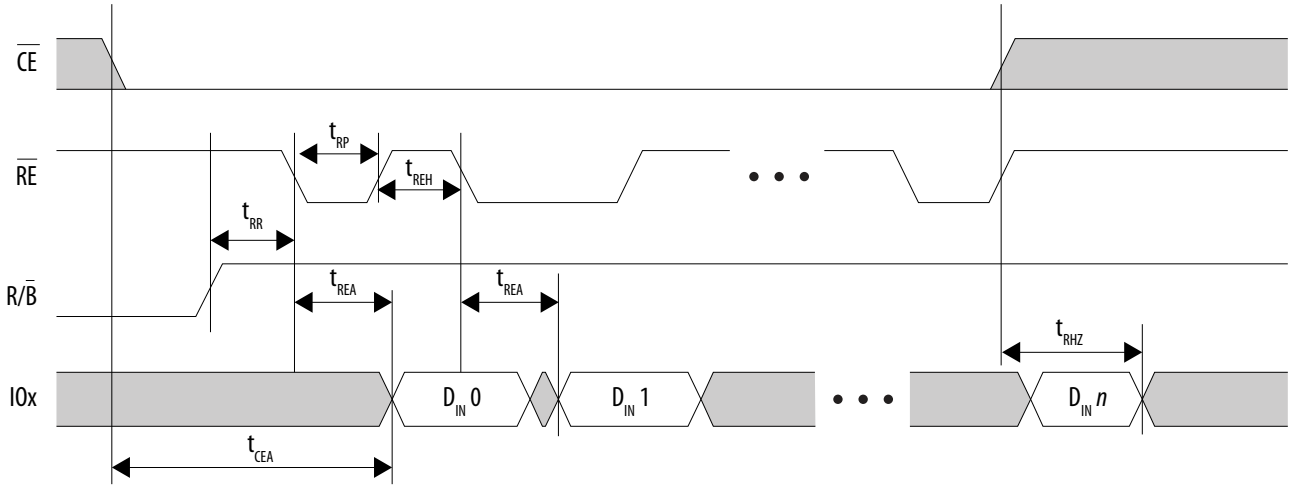


Figure 35. NAND SDR Read Status Timing Diagram

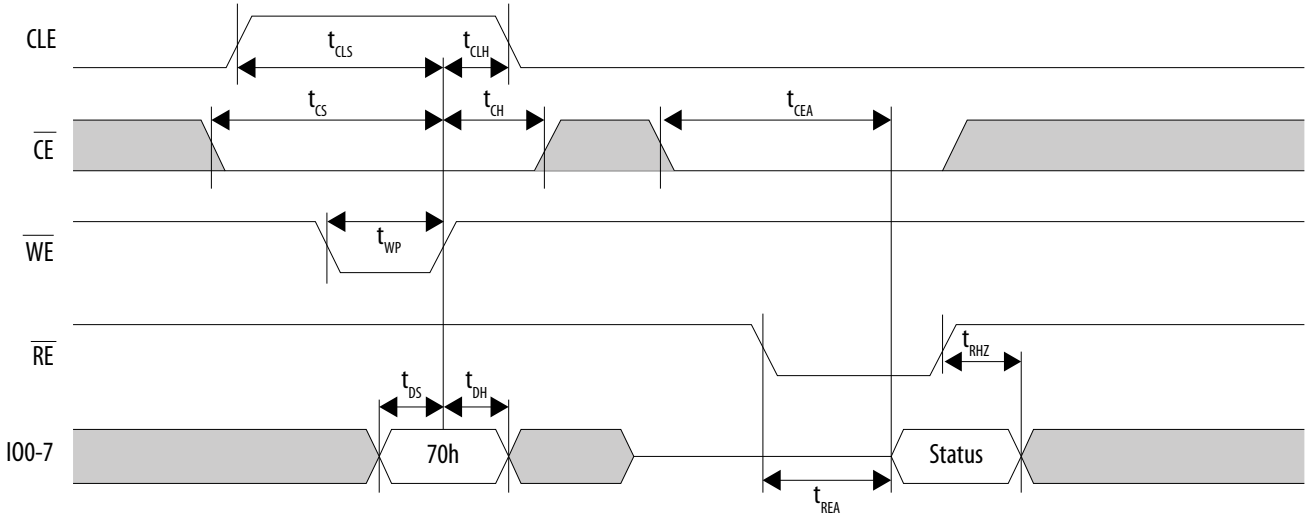


Figure 36. NAND SDR Read Status Enhanced Timing Diagram

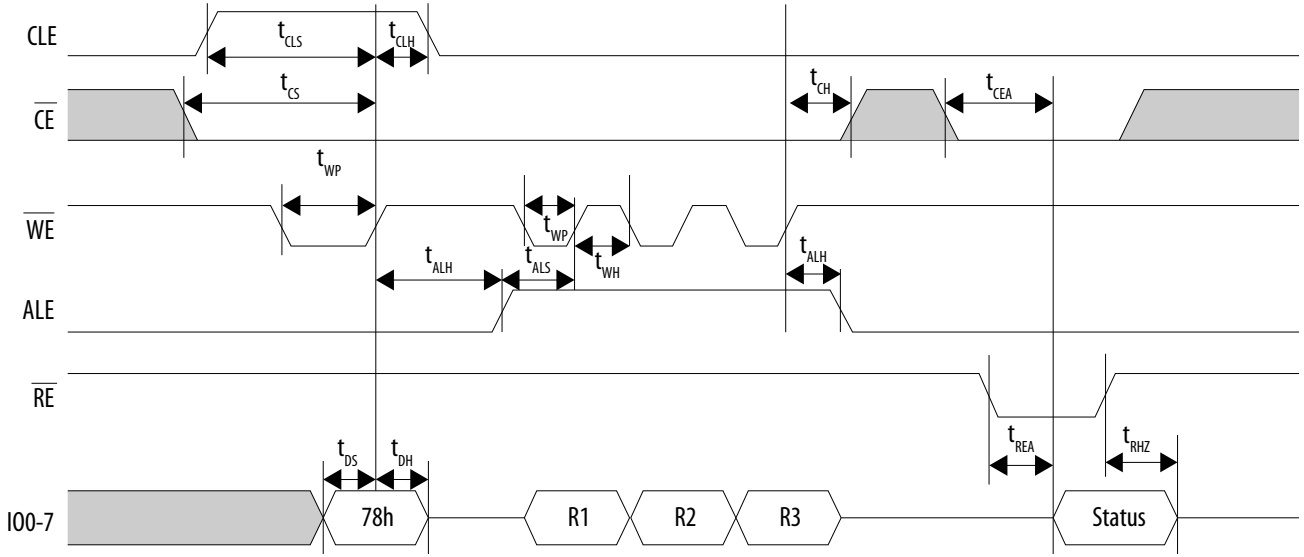


Table 89. HPS NAND DDR Timing Requirements

Compatible with the ONFI 1.x and 2.x specifications. Compatible with the Toggle 1.x and 2.x specifications. HPS I/O supports SDR, NV-DDR protocols up to 200 MT/s.

For specification status, see the *Data Sheet Status* table

Symbol	Description	100 MHz (200 MT/s)		
		Min	Max	Unit
t_{AC}	Access window of DQ[7:0] from CLK	3	25	ns
t_{ADL}	Address cycle to data loading time	400	—	ns
t_{CADf}	Command, address, data delay (fast) (command to command, address to address, command to	25	—	ns

continued...

Symbol	Description	100 MHz (200 MT/s)		
		Min	Max	Unit
	address, address to command, command/address to start of data)			
t_{CADs}	Command, address, data delay (slow) (command to command, address to address, command to address, address to command, command/address to start of data)	45	—	ns
t_{CAH}	Command/address DQ hold time	2	—	ns
t_{CALH}	W/R_n, CLE, and ALE hold time	2	—	ns
t_{CALS}	W/R_n, CLE, and ALE setup time	2	—	ns
t_{CAS}	Command/address DQ setup time	2	—	ns
t_{CEH}	CE_n high hold time	20	—	ns
t_{CH}	CE_n hold time	2	—	ns
$t_{CK(avg)}$ or t_{CK} (121)	Average clock cycle time	10	—	ns
$t_{CK(abs)}$	Absolute clock period, measured from rising edge to the next consecutive rising edge	$t_{CK(avg)} + t_{JIT(per)\ min}$	$t_{CK(avg)} + t_{JIT(per)\ max}$	ns
$t_{CKH(abs)}$ (122)	Clock cycle high	0.43	0.57	t_{CK}
$t_{CKL(abs)}$ (122)	Clock cycle low	0.43	0.57	t_{CK}
t_{CKWR}	Data output end to W/R_n high	RoundUp{[$t_{DQSCK(max)} + t_{CK}$] / t_{CK}}	—	t_{CK}

continued...

(121) $t_{CK(avg)}$ is the average clock period over any consecutive 200 cycles window.

(122) $t_{CKH(abs)}$ and $t_{CKL(abs)}$ include static offset and duty cycle jitter.

Symbol	Description	100 MHz (200 MT/s)		
		Min	Max	Unit
t_{CS3}	CE_n setup time for data input and data output after CE_n has been high for greater than 1 µs	75	—	ns
t_{CS}	CE_n setup time	15	—	ns
t_{DH}	Data hold time	0.9	—	ns
t_{DPZ}	Data input pause setup time	1.5	—	t_{DSC}
t_{DQSCK}	Access window of DQS from CLK	3	25	ns
t_{DQSD}	W/R_n low to DQS/DQ driven by device	0	18	ns
t_{DQSH} (123)	DQS input high pulse width	0.4	0.6	t_{CK} or t_{DSC4}
t_{DQSHZ} (124)	W/R_n high to DQS/DQ tri-state by device	—	20	ns
t_{DQSL} (123)	DQS input low pulse width	0.4	0.6	t_{CK} or t_{DSC4}
t_{DQSQ}	DQS-DQ skew, DQS to last DQ valid, per access	—	0.85	ns
t_{DQSS}	Data input to first DQS latching transition	0.75	1.25	t_{CK}
t_{DS}	Data setup time	0.9	—	ns
t_{DSC}	DQS cycle time	10	—	ns
t_{DSH}	DQS falling edge to CLK rising – hold time	0.2	—	t_{CK}
t_{DSS}	DQS falling edge to CLK rising – setup time	0.2	—	t_{CK}
t_{DVW}	Output data valid window	$t_{DVW} = t_{QH} - t_{DQSQ}$		ns

continued...

(123) t_{DQSL} and t_{DQSH} are relative to t_{CK} when CLK is running. If CLK is stopped during data input, then t_{DQSL} and t_{DQSH} are relative to t_{DSC}.

(124) t_{DQSHZ} is not referenced to a specific voltage level, but specifies when the device output is no longer driving.

Symbol	Description	100 MHz (200 MT/s)		
		Min	Max	Unit
t_{FEAT}	Busy time for Set Features and Get Features	—	1	µs
t_{HP}	Half-clock period	$t_{HP} = min(t_{CKL}, t_{CKH})$		ns
t_{ITC}	Interface and Timing Mode Change time	—	1	µs
$t_{JIT(per)}$	The deviation of a given $t_{CK(abs)}$ from $t_{CK(avg)}$	–0.5	0.5	ns
t_{QH}	DQ-DQS hold, DQS to first DQ to go non-valid, per access	$t_{QH} = t_{HP} - t_{QHS}$		ns
t_{QHS}	Data hold skew factor	—	1	ns
t_{RHW}	Data output cycle to command, address, or data input cycle	100	—	ns
t_{RR}	Ready to data output cycle (data only)	20	—	ns
t_{RST} (raw NAND)	Device reset time, measured from the falling edge of R/B_n to the rising edge of R/B_n	—	15/30/500	µs
t_{RST} (EZ NAND)(125)	Device reset time, measured from the falling edge of R/B_n to the rising edge of R/B_n	—	150/150/500	µs
t_{WB}	(WE_n high or CLK rising edge) to SR[6] low	—	100	ns
t_{WHR}	Command, address, or data input cycle to data output cycle	80	—	ns
t_{WPRE}	DQS write preamble	1.5	—	t_{CK}

continued...

(125) If the reset is invoked using a Reset (FFh) command then the EZ NAND device has 250 ms to complete the reset operation regardless of the timing mode. If the reset is invoked using Synchronous Reset (FCh) or a Reset LUN (FAh) command then the values are as shown.

Symbol	Description	100 MHz (200 MT/s)		
		Min	Max	Unit
t_{WPST}	DQS write postamble	1.5	—	t_{CK}
t_{WRCK}	W/R_n low to data output cycle	20	—	ns
t_{WW}	WP_n transition to command cycle	100	—	ns

Figure 37. NAND DDR Command Cycle Timing Diagram

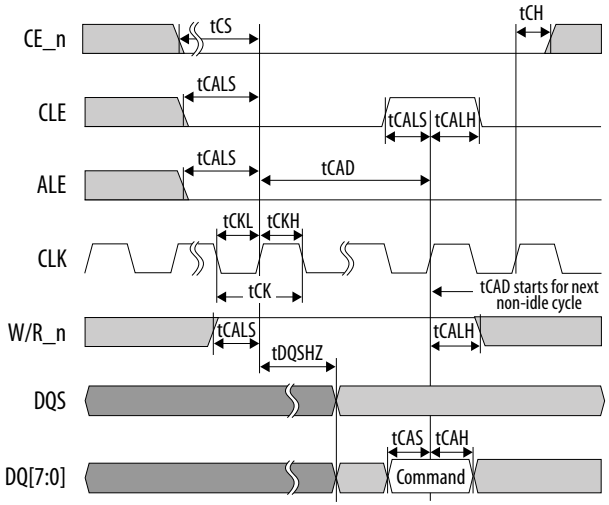


Figure 38. NAND DDR Address Cycle Timing Diagram

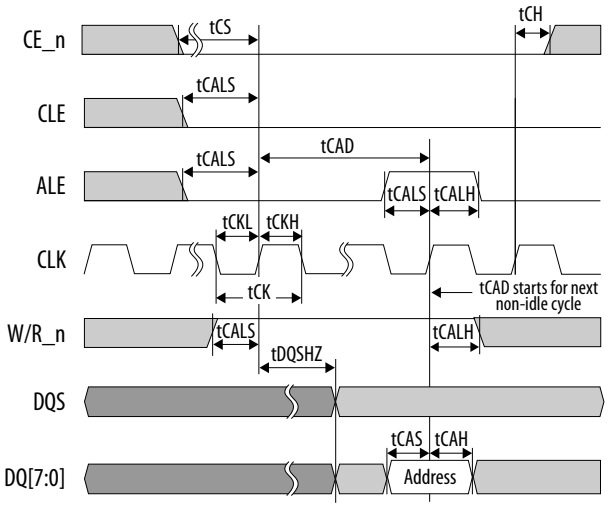


Figure 39. NAND DDR Data Input Cycle Timing Diagram

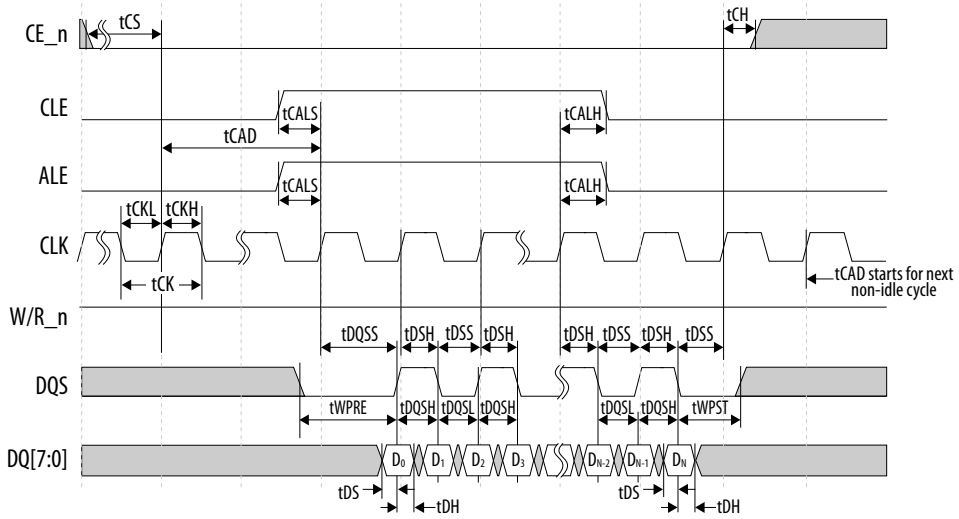


Figure 40. NAND DDR Data Input Cycle Timing Diagram (CLK Stopped)

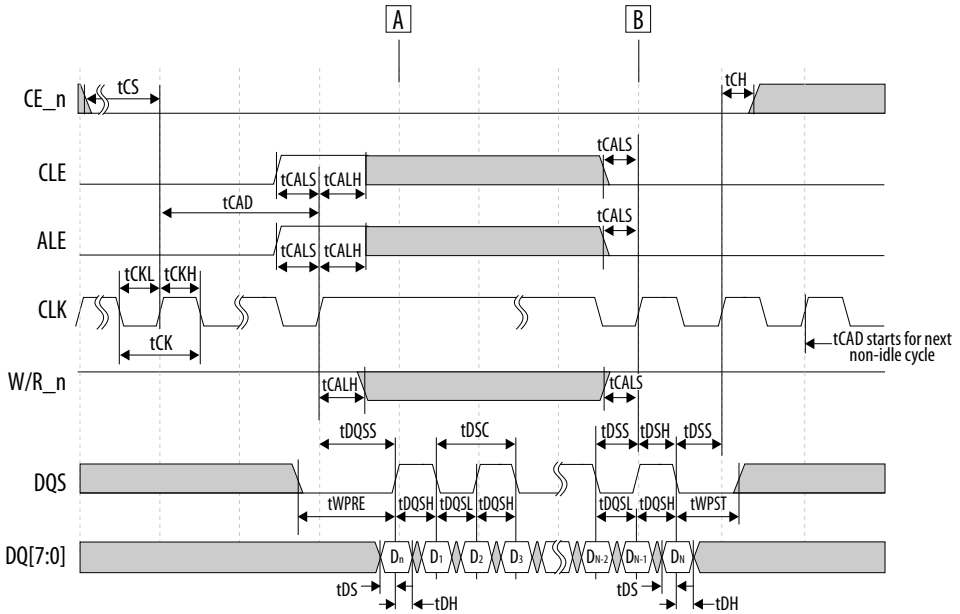


Figure 41. NAND DDR Data Input Cycle Timing Diagram (CLK Stopped with Data Pause)

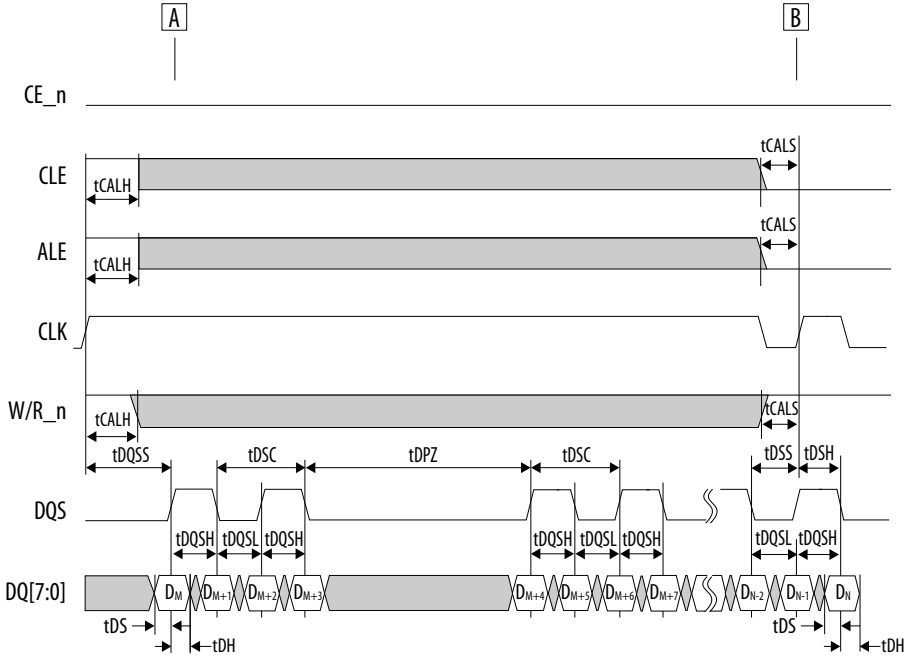


Figure 42. NAND DDR Data Output Cycle Timing Diagram

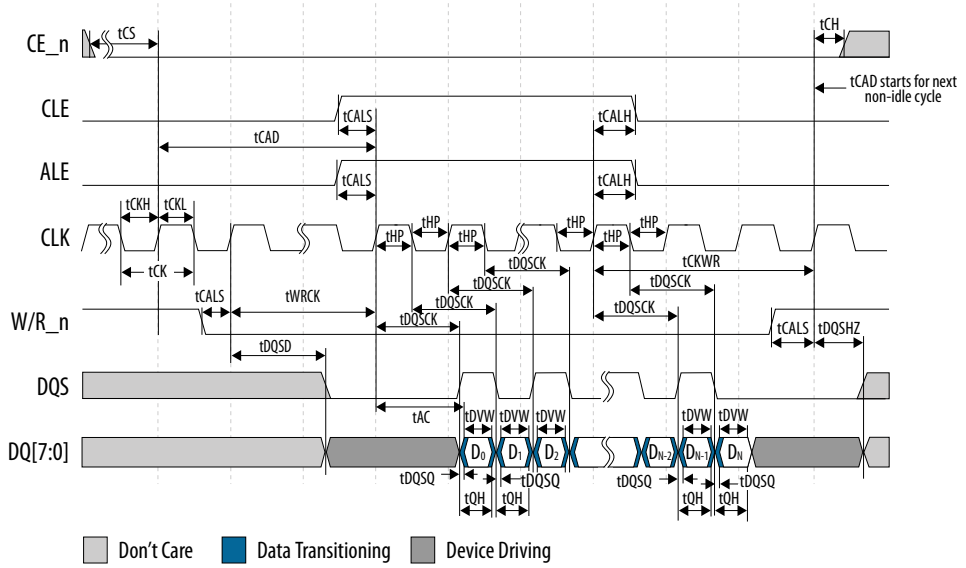


Figure 43. NAND DDR W/R_n Timing Diagram

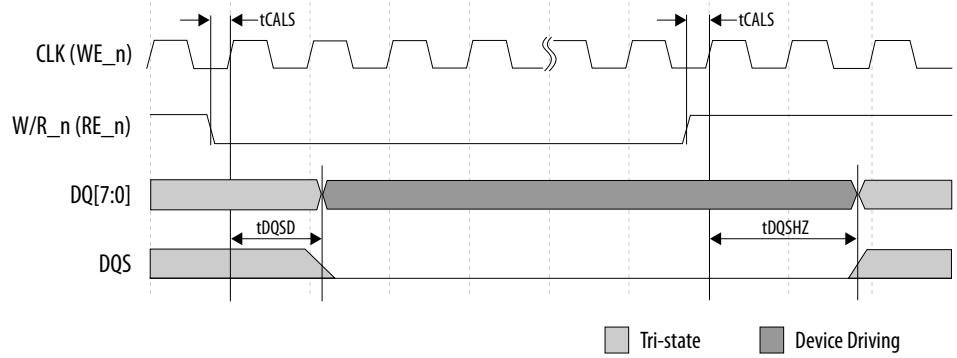
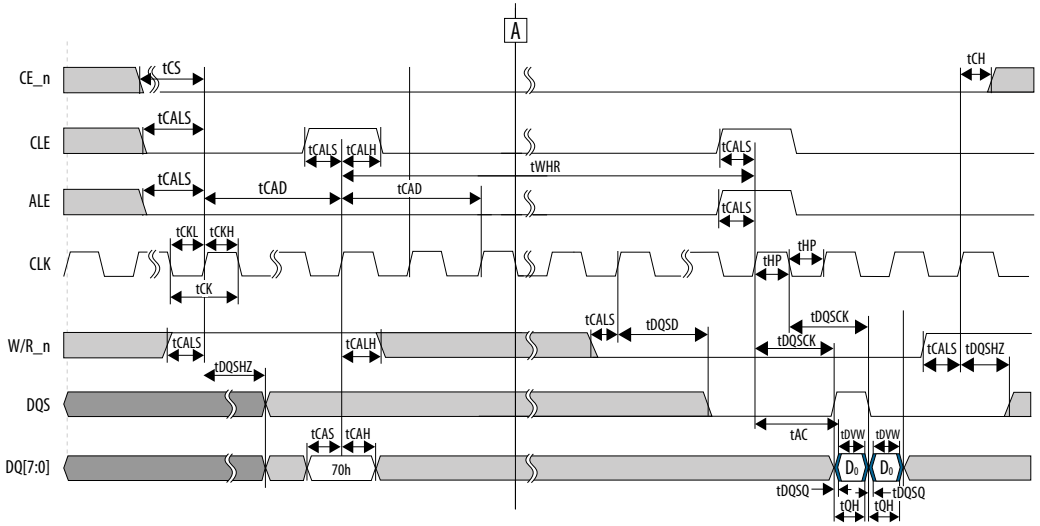


Figure 44. NAND DDR Read Status Including tWHR and tCAD Timing Diagram



HPS Trace Timing Characteristics

Table 90. Trace Timing Requirements

To increase the trace bandwidth, Altera recommends routing the trace interface to the FPGA in the HPS Platform Designer component. The FPGA trace interface offers a 64-bit single data rate path that can be converted to double data rate to minimize FPGA I/O usage.

Depending on the trace module that you connect to the HPS trace interface, you may need to include board termination to achieve the maximum sampling speed possible. Refer to your trace module data sheet for termination recommendations.

Most trace modules implement programmable clock and data skew to improve trace data timing margins. Alternatively, you can change the clock-to-data timing relationship with the HPS programmable I/O delay.

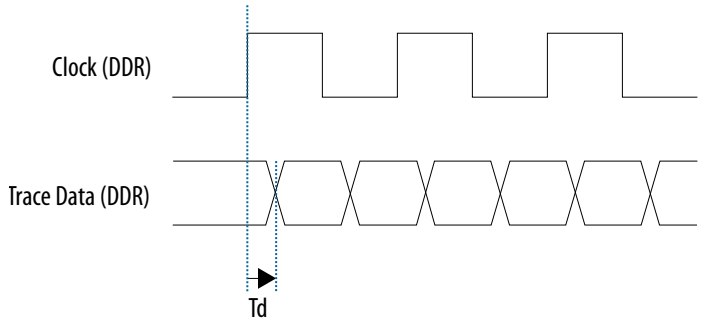
For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
F_{clk}	Trace clock frequency	—	—	200	MHz
T_{clk}	Trace clock period	5	—	—	ns

continued...

Symbol	Description	Min	Typ	Max	Unit
T_{clk_jitter}	Trace clock output jitter	—	—	2	%
$T_{dutycycle}$	Trace clock maximum duty cycle	45	50	55	%
T_d	T_{clk} to D0–D15 output data delay	–0.5	—	1.3	ns

Figure 45. Trace Timing Diagram



HPS GPIO Interface

The general-purpose I/O (GPIO) interface has debounce circuitry included to remove signal glitches. The debounce clock frequency ranges from 125 Hz to 32 kHz. The minimum pulse width is 1 debounce clock cycle and the minimum detectable GPIO pulse width is 62.5 µs (at 32 kHz).

If the external signal is driven into the GPIO for less than one clock cycle, the external signal is filtered. If the external signal is between one and two clock cycles, the external signal may or may not be filtered depending on the phase of the signal. If the external signal is more than two clock cycles, the external signal is not filtered.

The GPIO modules provided in the HPS include optional debounce capabilities. The external signal can be debounced to remove any spurious glitches that are less than one period of the external debouncing clock, `gpio_db_clk`.

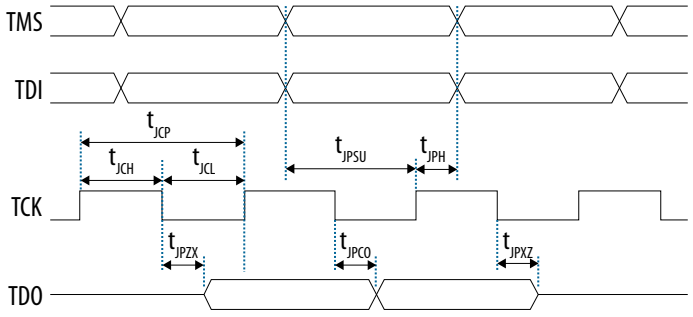
HPS JTAG Timing Characteristics

Table 91. HPS JTAG Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
F_{JCP}	TCK clock frequency	—	—	33.33	MHz
t_{JCP}	TCK clock period	30	—	—	ns
t_{JCH}	TCK clock high time	20	—	—	ns
t_{JCL}	TCK clock low time	20	—	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	5	—	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	5	—	—	ns
t_{JPH}	JTAG port hold time	0.5	—	—	ns
t_{JPCO}	JTAG port clock to output	0	—	8	ns
t_{JPZX}	JTAG port high impedance to valid output	—	—	10	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	—	10	ns

Figure 46. HPS JTAG Timing Diagram



HPS Programmable I/O Timing Characteristics

Table 92. HPS Programmable I/O Delay (Output Path)

For specification status, see the *Data Sheet Status* table

Name	output_val_en	output_val	Description	Min	Typ	Max	Unit
ZERO_CHAIN_DELAY	0	0	Intrinsic I/O delay. Bypasses the delay chain	—	0	—	ps
CHAIN_DELAY	1	0	Intrinsic I/O delay + Minimum + 0 × Chain Delay	—	0	—	ps
ONE_CHAIN_DELAY	1	1	Intrinsic I/O delay + Minimum + 1 × Chain Delay	—	208	—	ps
TWO_CHAIN_DELAY	1	2	Intrinsic I/O delay + Minimum + 2 × Chain Delay	—	353	—	ps
THREE_CHAIN_DELAY	1	3	Intrinsic I/O delay + Minimum + 3 × Chain Delay	—	413	—	ps
FOUR_CHAIN_DELAY	1	4	Intrinsic I/O delay + Minimum + 4 × Chain Delay	—	524	—	ps
FIVE_CHAIN_DELAY	1	5	Intrinsic I/O delay + Minimum + 5 × Chain Delay	—	623	—	ps
SIX_CHAIN_DELAY	1	6	Intrinsic I/O delay + Minimum + 6 × Chain Delay	—	744	—	ps
SEVEN_CHAIN_DELAY	1	7	Intrinsic I/O delay + Minimum + 7 × Chain Delay	—	878	—	ps
EIGHT_CHAIN_DELAY	1	8	Intrinsic I/O delay + Minimum + 8 × Chain Delay	—	977	—	ps

continued...

Name	output_val_en	output_val	Description	Min	Typ	Max	Unit
NINE_CHAIN_DELAY	1	9	Intrinsic I/O delay + Minimum + 9 × Chain Delay	—	1,067	—	ps
TEN_CHAIN_DELAY	1	10	Intrinsic I/O delay + Minimum + 10 × Chain Delay	—	1,170	—	ps
ELEVEN_CHAIN_DELAY	1	11	Intrinsic I/O delay + Minimum + 11 × Chain Delay	—	1,309	—	ps
TWELVE_CHAIN_DELAY	1	12	Intrinsic I/O delay + Minimum + 12 × Chain Delay	—	1,366	—	ps
THIRTEEN_CHAIN_DELAY	1	13	Intrinsic I/O delay + Minimum + 13 × Chain Delay	—	1,499	—	ps
FOURTEEN_CHAIN_DELAY	1	14	Intrinsic I/O delay + Minimum + 14 × Chain Delay	—	1,604	—	ps
FIFTEEN_CHAIN_DELAY	1	15	Intrinsic I/O delay + Minimum + 15 × Chain Delay	—	1,760	—	ps
—	1	[16:30]	INVALID	—	—	—	—
—	2	—	INVALID	—	—	—	—
—	3	[0:15]	INVALID	—	—	—	—
SIXTEEN_CHAIN_DELAY	3	16	Intrinsic I/O delay + Minimum + 16 × Chain Delay	—	1,994	—	ps
SEVENTEEN_CHAIN_DELAY	3	17	Intrinsic I/O delay + Minimum + 17 × Chain Delay	—	2,038	—	ps
EIGHTEEN_CHAIN_DELAY	3	18	Intrinsic I/O delay + Minimum + 18 × Chain Delay	—	2,169	—	ps

continued...

Name	output_val_en	output_val	Description	Min	Typ	Max	Unit
NINETEEN_CHAIN_DELAY	3	19	Intrinsic I/O delay + Minimum + 19 × Chain Delay	—	2,260	—	ps
TWENTY_CHAIN_DELAY	3	20	Intrinsic I/O delay + Minimum + 20 × Chain Delay	—	2,433	—	ps
TWENTYONE_CHAIN_DELAY	3	21	Intrinsic I/O delay + Minimum + 21 × Chain Delay	—	2,476	—	ps
TWENTYTWO_CHAIN_DELAY	3	22	Intrinsic I/O delay + Minimum + 22 × Chain Delay	—	2,645	—	ps
TWENTYTHREE_CHAIN_DELAY	3	23	Intrinsic I/O delay + Minimum + 23 × Chain Delay	—	2,684	—	ps
TWENTYFOUR_CHAIN_DELAY	3	24	Intrinsic I/O delay + Minimum + 24 × Chain Delay	—	2,858	—	ps
TWENTYFIVE_CHAIN_DELAY	3	25	Intrinsic I/O delay + Minimum + 25 × Chain Delay	—	2,907	—	ps
TWENTYSIX_CHAIN_DELAY	3	26	Intrinsic I/O delay + Minimum + 26 × Chain Delay	—	3,054	—	ps
TWENTYSEVEN_CHAIN_DELAY	3	27	Intrinsic I/O delay + Minimum + 27 × Chain Delay	—	3,123	—	ps
TWENTYEIGHT_CHAIN_DELAY	3	28	Intrinsic I/O delay + Minimum + 28 × Chain Delay	—	3,259	—	ps
TWENTYNINE_CHAIN_DELAY	3	29	Intrinsic I/O delay + Minimum + 29 × Chain Delay	—	3,301	—	ps
THIRTY_CHAIN_DELAY	3	30	Intrinsic I/O delay + Minimum + 30 × Chain Delay	—	3,488	—	ps

Table 93. HPS Programmable I/O Delay (Input Path)

For specification status, see the *Data Sheet Status* table

Name	input_val_en	input_val	Description	Min	Typ	Max	Unit
ZERO_CHAIN_DELAY	0	0	Intrinsic I/O delay. Bypasses the delay chain	—	0	—	ps
CHAIN_DELAY	1	0	Intrinsic I/O delay + Minimum + 0 × Chain Delay	—	0	—	ps
ONE_CHAIN_DELAY	1	1	Intrinsic I/O delay + Minimum + 1 × Chain Delay	—	208	—	ps
TWO_CHAIN_DELAY	1	2	Intrinsic I/O delay + Minimum + 2 × Chain Delay	—	353	—	ps
THREE_CHAIN_DELAY	1	3	Intrinsic I/O delay + Minimum + 3 × Chain Delay	—	413	—	ps
FOUR_CHAIN_DELAY	1	4	Intrinsic I/O delay + Minimum + 4 × Chain Delay	—	524	—	ps
FIVE_CHAIN_DELAY	1	5	Intrinsic I/O delay + Minimum + 5 × Chain Delay	—	623	—	ps
SIX_CHAIN_DELAY	1	6	Intrinsic I/O delay + Minimum + 6 × Chain Delay	—	744	—	ps
SEVEN_CHAIN_DELAY	1	7	Intrinsic I/O delay + Minimum + 7 × Chain Delay	—	878	—	ps
EIGHT_CHAIN_DELAY	1	8	Intrinsic I/O delay + Minimum + 8 × Chain Delay	—	977	—	ps
NINE_CHAIN_DELAY	1	9	Intrinsic I/O delay + Minimum + 9 × Chain Delay	—	1,067	—	ps

continued...

Name	input_val_en	input_val	Description	Min	Typ	Max	Unit
TEN_CHAIN_DELAY	1	10	Intrinsic I/O delay + Minimum + 10 × Chain Delay	—	1,170	—	ps
ELEVEN_CHAIN_DELAY	1	11	Intrinsic I/O delay + Minimum + 11 × Chain Delay	—	1,309	—	ps
TWELVE_CHAIN_DELAY	1	12	Intrinsic I/O delay + Minimum + 12 × Chain Delay	—	1,366	—	ps
THIRTEEN_CHAIN_DELAY	1	13	Intrinsic I/O delay + Minimum + 13 × Chain Delay	—	1,499	—	ps
FOURTEEN_CHAIN_DELAY	1	14	Intrinsic I/O delay + Minimum + 14 × Chain Delay	—	1,604	—	ps
FIFTEEN_CHAIN_DELAY	1	15	Intrinsic I/O delay + Minimum + 15 × Chain Delay	—	1,760	—	ps
—	1	[16:30]	INVALID	—	—	—	—
—	2	—	INVALID	—	—	—	—
—	3	[0:15]	INVALID	—	—	—	—
SIXTEEN_CHAIN_DELAY	3	16	Intrinsic I/O delay + Minimum + 16 × Chain Delay	—	1,994	—	ps
SEVENTEEN_CHAIN_DELAY	3	17	Intrinsic I/O delay + Minimum + 17 × Chain Delay	—	2,038	—	ps
EIGHTEEN_CHAIN_DELAY	3	18	Intrinsic I/O delay + Minimum + 18 × Chain Delay	—	2,169	—	ps
NINETEEN_CHAIN_DELAY	3	19	Intrinsic I/O delay + Minimum + 19 × Chain Delay	—	2,260	—	ps

continued...

Name	input_val_en	input_val	Description	Min	Typ	Max	Unit
TWENTY_CHAIN_DELAY	3	20	Intrinsic I/O delay + Minimum + 20 × Chain Delay	—	2,433	—	ps
TWENTYONE_CHAIN_DELAY	3	21	Intrinsic I/O delay + Minimum + 21 × Chain Delay	—	2,476	—	ps
TWENTYTWO_CHAIN_DELAY	3	22	Intrinsic I/O delay + Minimum + 22 × Chain Delay	—	2,645	—	ps
TWENTYTHREE_CHAIN_DELAY	3	23	Intrinsic I/O delay + Minimum + 23 × Chain Delay	—	2,684	—	ps
TWENTYFOUR_CHAIN_DELAY	3	24	Intrinsic I/O delay + Minimum + 24 × Chain Delay	—	2,858	—	ps
TWENTYFIVE_CHAIN_DELAY	3	25	Intrinsic I/O delay + Minimum + 25 × Chain Delay	—	2,907	—	ps
TWENTYSIX_CHAIN_DELAY	3	26	Intrinsic I/O delay + Minimum + 26 × Chain Delay	—	3,054	—	ps
TWENTYSEVEN_CHAIN_DELAY	3	27	Intrinsic I/O delay + Minimum + 27 × Chain Delay	—	3,123	—	ps
TWENTYEIGHT_CHAIN_DELAY	3	28	Intrinsic I/O delay + Minimum + 28 × Chain Delay	—	3,259	—	ps
TWENTYNINE_CHAIN_DELAY	3	29	Intrinsic I/O delay + Minimum + 29 × Chain Delay	—	3,301	—	ps
THIRTY_CHAIN_DELAY	3	30	Intrinsic I/O delay + Minimum + 30 × Chain Delay	—	3,488	—	ps

You can program the number of delay steps by adjusting the I/O Delay register (`io0_delay` through `io47_delay` for I/Os 0 through 47).

Configuration Specifications

General Configuration Timing Specifications

Table 94. General Configuration Timing Specifications

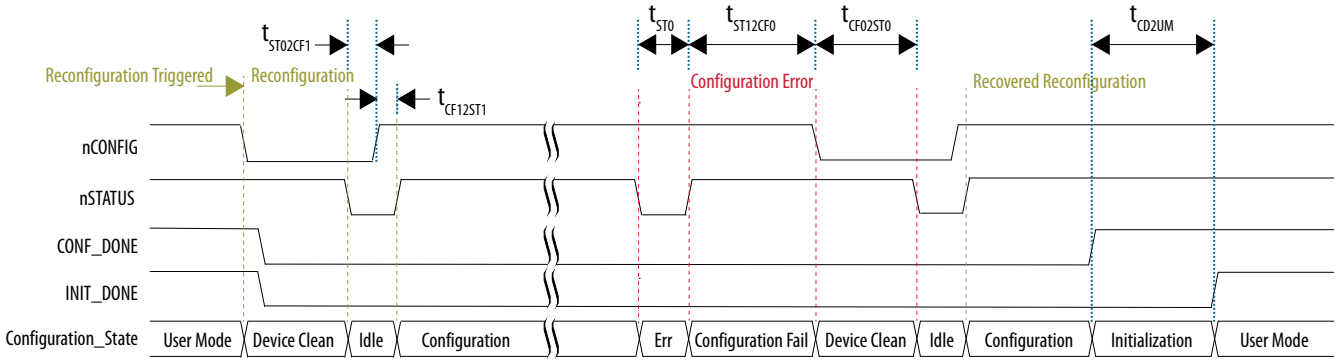
For specification status, see the *Data Sheet Status* table

Symbol	Description	Requirement		Unit
		Min	Max	
$t_{CF12ST1}$	nCONFIG high to nSTATUS high	—	20	ms
$t_{CF02ST0}$ (126)	nCONFIG low to nSTATUS low	—	400	ms
t_{ST0}	nSTATUS low pulse during configuration error	0.5	10	ms
t_{CD2UM} (127)	CONF_DONE high to user mode	—	5	ms
$t_{ST12CF0}$	Minimum time to drive nCONFIG from high to low after nSTATUS transitions from low to high	0	—	ms
$t_{ST02CF1}$	Minimum time to drive nCONFIG from low to high after nSTATUS transitions from high to low	0	—	ms

(126) You need to drive nCONFIG low pulse by referring to maximum value if nSTATUS cannot be monitored by host.

(127) This specification is the initialization time that indicates the time from CONF_DONE signal goes high to INIT_DONE signal goes high.

Figure 47. General Configuration Timing Diagram



POR Specifications

POR delay is defined as the delay between the last power rail monitored by the POR circuitry from Group 2B to reach the minimum operating condition voltage to the time your device is ready to begin configuration.

Table 95. POR Delay Specifications

For specification status, see the *Data Sheet Status* table

POR Delay	Minimum	Maximum	Unit
AS (Normal mode), AVST ×8, AVST ×16	11.5	20.2	ms
AS (Fast mode)	1.5	7.6	ms

External Configuration Clock Source Requirements

Table 96. External Configuration Clock Source (OSC_CLK_1) Clock Input Requirements

For specification status, see the *Data Sheet Status* table

Description	External Clock Source	Min	Typ	Max	Unit
Clock input frequency(128)	Powered by V_{CCIO_SDM}		25/100/125		MHz
Clock input peak-to-peak period jitter tolerance		—	—	2	%
Clock input duty cycle		45	50	55	%

JTAG Configuration Timing

Table 97. JTAG Timing Parameters and Values

For specification status, see the *Data Sheet Status* table

Symbol	Description	Requirement		Unit
		Minimum	Maximum	
t_{JCP}	TCK clock period	30	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$ (129)	TDI JTAG port setup time	2	—	ns
$t_{JPSU\ (TMS)}$ (129)	TMS JTAG port setup time	3	—	ns
t_{JPH} (129)	JTAG port hold time	5	—	ns

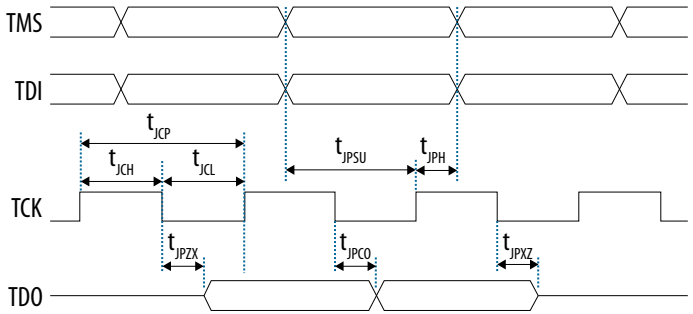
continued...

(128) The acceptable clock frequencies are 25 MHz, 100 MHz, and 125 MHz only. You must match the external configuration clock frequency on the OSC_CLK_1 pin to the configuration clock source assignment in the Quartus Prime software. Other frequencies in the range are not supported.

(129) For boundary-scan testing, the TMS and TDI JTAG ports minimum setup time and hold time are 7 ns.

Symbol	Description	Requirement		Unit
		Minimum	Maximum	
t_{JPCO}	JTAG port clock to output	—	7(130)	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14	ns

Figure 48. JTAG Timing Diagram



AS Configuration Timing

Table 98. AS Timing Parameters

Altera recommends performing trace length matching for nCSO and AS_DATA pins to AS_CLK to minimize the skew.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{clk} (131)	AS_CLK clock period	—	6.02	—	ns
$T_{dutycycle}$	AS_CLK duty cycle	45	50	55	%

continued...

(130) Capacitance loading at 10 pF.

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{dcsfrs}	AS_nCSO[3:0] asserted to first AS_CLK edge	8.5(132)	—	—	ns
T_{dcslst}	Last AS_CLK edge to AS_nCSO[3:0] deasserted	6.8(132)	—	—	ns
T_{do} (133)	AS_DATA[3:0] output delay	–0.6	—	0.6	ns
T_{ext_delay} (134) (135) (136)	Total external propagation delay on AS signals	—	—	13.5	ns

continued...

(131) AS_CLK f_{MAX} has dependency on the maximum board loading. For AS single device configuration or AS using multiple serial flash devices configuration, use the equations in T_{do} and T_{ext_delay} notes to ensure your board has sufficient timing margin to meet flash setup/hold time specifications and AS timing specifications in this data sheet. For AS using multiple serial flash devices, refer to the *Configuration User Guide* for the recommended AS_CLK frequency and maximum board loading.

(132) AS operating at maximum clock frequency = 166 MHz. The delay is larger when operating at AS clock frequency lower than 166 MHz.

(133) Load capacitance for DCLK = 10 pF and AS_DATA = 18 pF. Altera recommends obtaining the T_{do} for a given link (including receiver, transmission lines, connectors, termination resistors, and other components) through IBIS or HSPIC simulation. To analyze flash setup time,

- $T_{su} = T_{clk}/2 - T_{do(max)} + T_{bd\_clk} - T_{bd\_data(max)}$
- $T_{ho} = T_{clk}/2 + T_{do(min)} - T_{bd\_clk} + T_{bd\_data(min)}$

(134) $T_{ext\_delay} = T_{bd\_clk} + T_{co} + T_{bd\_data} + T_{add}$

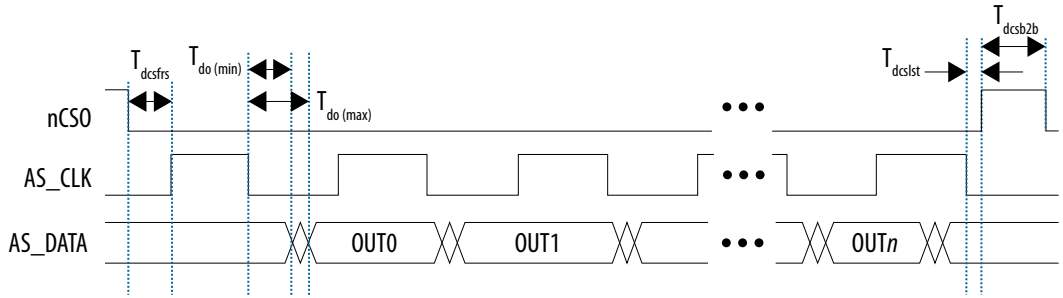
- T_{bd_clk}: Propagation delay for AS_CLK between FPGA and flash device.
- T_{co}: Output hold time and clock low to output valid of flash device. This delay must be used to ensure T_{ext_delay} is within the minimum and maximum specification values.
- T_{bd_data}: Propagation delay for AS_DATA bus between FPGA and flash device.
- T_{add}: Propagation delay for active/passive components on AS_DATA interfaces.

(135) T_{ext_delay} specification is based on AS_CLK = 166 MHz. The value can be larger at lower AS_CLK frequency.

(136) Meeting T_{ext_delay} timing specifications indicates that the AS_DATA setup/hold timing is met.

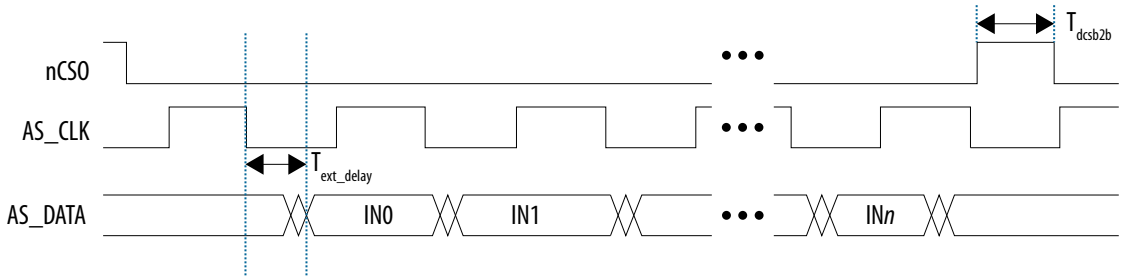
Symbol	Description	Minimum	Typical	Maximum	Unit
T_{dcsb2b}	Minimum delay of slave select deassertion between two back-to-back transfers	62	—	—	ns
Skew (AS_CLK – AS_nCSO)	Maximum skew tolerance between nCSO and AS_CLK	$T_{su\_ncso} - T_{dcsfrs} < Skew\ (AS\_CLK - AS\_nCSO) < AS\_CLK/2 + T_{dcslst} - T_{ho\_ncso}$ (137)			ns
Skew (AS_CLK – AS_DATA)	Maximum skew tolerance between AS_CLK and AS_DATA	$-AS\_CLK/2 + T_{do(max)} + T_{su} < Skew\ (AS\_CLK - AS\_DATA) < AS\_CLK/2 + T_{do(min)} - T_{ho}$ (137)			ns

Figure 49. AS Configuration Serial Output Timing Diagram



(137)
- T_{su} = Data setup time required by the quad SPI flash. Refer to your quad SPI flash datasheet.
- T_{ho} = Data hold time required by the quad SPI flash. Refer to your quad SPI flash datasheet.
- T_{do} = AS_DATA[3:0] output delay. Refer to the specification in this table.
- AS_CLK = AS_CLK clock period.
- T_{su_ncso} = Chip select setup time required by the quad SPI flash. Refer to your quad SPI flash datasheet.
- T_{ho_ncso} = Chip select hold time required by the quad SPI flash. Refer to your quad SPI flash datasheet.
- T_{dcsfrs} = AS_nCSO[3:0] asserted to first AS_CLK edge. Refer to the specification in this table.
- T_{dcslst} = Last AS_CLK edge to AS_nCSO[3:0] deasserted. Refer to the specification in this table.

Figure 50. AS Configuration Serial Input Timing Diagram



Avalon Streaming Configuration Timing

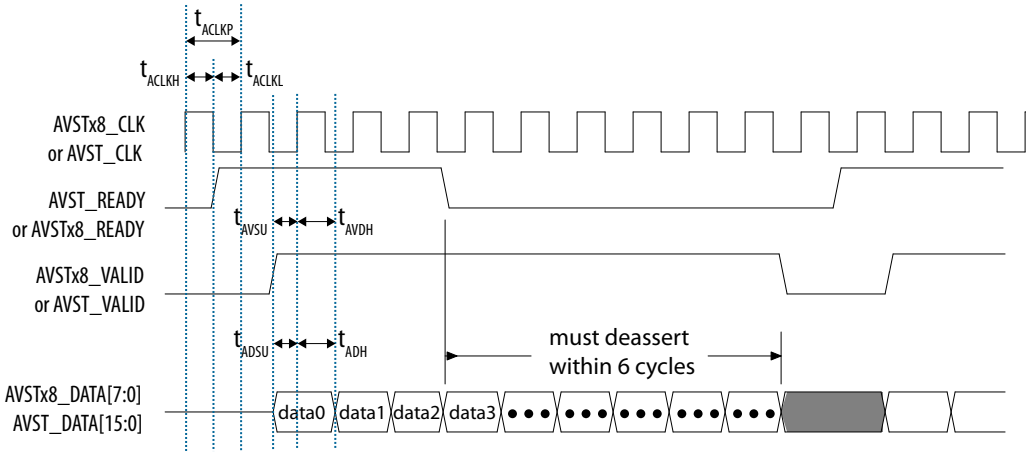
Table 99. Avalon Streaming Timing Parameters for ×8 and ×16 Configurations

For specification status, see the *Data Sheet Status* table

Symbol	Description	Minimum	Unit
t_{ACLKH}	AVST_CLK high time	3.6	ns
t_{ACLKL}	AVST_CLK low time	3.6	ns
t_{ACLKP}	AVST_CLK period	8	ns
t_{ADSU} (138)	AVST_DATA setup time before rising edge of AVST_CLK	2.1	ns
t_{ADH} (138)	AVST_DATA hold time after rising edge of AVST_CLK	0.1	ns
t_{AVSU}	AVST_VALID setup time before rising edge of AVST_CLK	2.1	ns
t_{AVDH}	AVST_VALID hold time after rising edge of AVST_CLK	0	ns

(138) Data sampled by the FPGA (sink) at the next rising clock edge.

Figure 51. Avalon Streaming Configuration Timing Diagram



Configuration Bit Stream Sizes

Table 100. Configuration Bit Stream Sizes

Configuration bit stream sizes shown in this table are based on worst-case scenarios. The sizes are typically substantially smaller because of the use of the Altera bit stream compression. The Altera bit stream compression efficiency has dependency on your design complexity.

128 Mb quad SPI flash size is adequate to store the periphery image.

For specification status, see the *Data Sheet Status* table

Variant	Compressed Configuration Bit Stream Size (Mbits)
A3C 025, A3C 050, A3C 065	38
A3C 100, A3C 135	62

I/O Timing

I/O timing data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the timing analysis. You may generate the I/O timing report manually using the Timing Analyzer.

The Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Programmable IOE Delay

Table 101. Programmable IOE Delay Specifications

For specification status, see the *Data Sheet Status* table

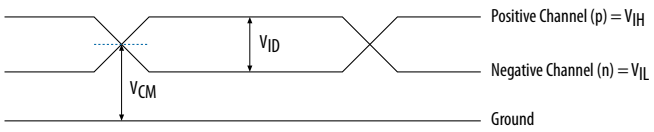
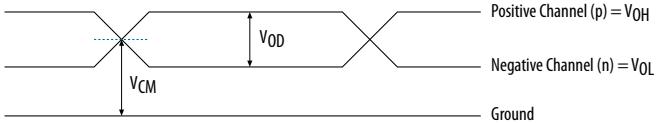
Parameter	Maximum Offset	Minimum Offset	Fast Model	Slow Model		Unit
			Extended, Industrial	–E6S, –I6S	-E7S, -I7S	
Input Delay Chain (INPUT_DELAY_CHAIN)	63	0	1.798	4.906	6.304	ns
Output Delay Chain (OUTPUT_DELAY_CHAIN)	15	0	0.435	1.204	1.554	ns
Output Enable Delay Chain (OUTPUT_EENABLE_DELAY_CHAIN)	15	0	0.436	1.204	1.553	ns

Glossary

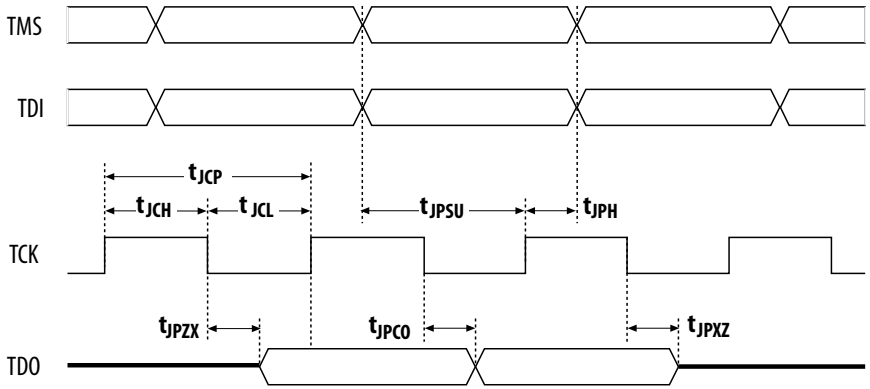
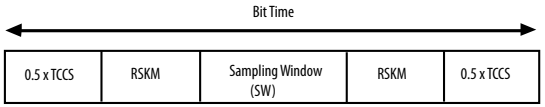
Table 102. Glossary

Term	Definition
Differential I/O Standards	Receiver Input Waveforms

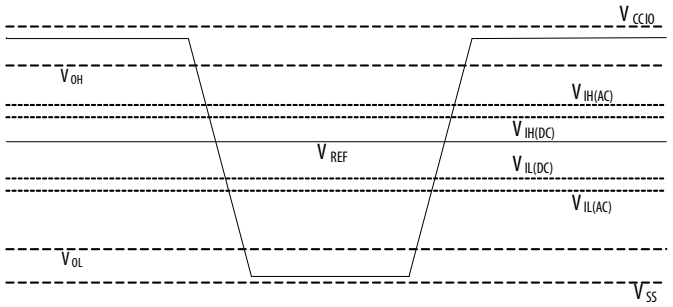
continued...

Term	Definition
	Single-Ended Waveform  **Differential Waveform**  Transmitter Output Waveforms **Single-Ended Waveform**  **Differential Waveform** 
f_{HSCLK}	I/O PLL input clock frequency.
f_{HSDR}	LVDS SERDES block—maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
$f_{HSDRDPA}$	LVDS SERDES block—maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
J (SERDES factor)	LVDS SERDES block—deserialization factor (width of parallel data bus).
JTAG Timing Specifications	JTAG Timing Specifications:

continued...

Term	Definition
	
R_L	Receiver differential input discrete resistor (external to the device).
Sampling window (SW)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown: 
Single-ended voltage referenced I/O standard	The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing. Single-Ended Voltage Referenced I/O Standard

continued...

Term	Definition
	
t_C	High-speed receiver/transmitter input and output clock period.
TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
t_{DUTY}	LVDS SERDES block—duty cycle on high-speed transmitter output clock.
t_{FALL}	Signal high-to-low transition time (80–20%).
t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input.
t_{OUTPJ_IO}	Period jitter on the GPIO driven by a PLL.
t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL.
t_{RISE}	Signal low-to-high transition time (20–80%).
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w).
$V_{CM(DC)}$	DC Common mode input voltage.
V_{ICM}	Input Common mode voltage—the common mode of the differential signal at the receiver.
$V_{ICM(DC)}$	$V_{CM(DC)}$ DC Common mode input voltage.
V_{ID}	Input differential voltage swing—the difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
$V_{DIF(AC)}$	AC differential input voltage—minimum AC input differential voltage required for switching.

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Term	Definition
$V_{DIF(DC)}$	DC differential input voltage—minimum DC input differential voltage required for switching.
V_{IH}	Voltage input high—the minimum positive voltage applied to the input which is accepted by the device as a logic high.
$V_{IH(AC)}$	High-level AC input voltage.
$V_{IH(DC)}$	High-level DC input voltage.
V_{IL}	Voltage input low—the maximum positive voltage applied to the input which is accepted by the device as a logic low.
$V_{IL(AC)}$	Low-level AC input voltage.
$V_{IL(DC)}$	Low-level DC input voltage.
V_{OCM}	Output Common mode voltage—the common mode of the differential signal at the transmitter.
V_{OD}	Output differential voltage swing—the difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter.
V_{SWING}	Differential input voltage.
V_{OX}	Output differential cross point voltage.
$V_{IX(AC)}$	V_{IX} Input differential cross point voltage.
W	LVDS SERDES block—Clock Boost Factor.

Document Revision History for the Agilex 3 FPGAs and SoCs Device Data Sheet

Document Version	Changes
2025.10.27	• Updated the status of A3C 100/135 device M16A and B18A packages to Final in the *Data Sheet Status for Agilex 3 FPGAs and SoCs* table. • Updated the status of A3C 100/135 device (B18A and B23C packages) and A3C 025/050/065 device (B18A and B18B packages) to Preliminary in the *Data Sheet Status for Agilex 3 FPGAs and SoCs* table. • Updated specifications in the *HPS Internal Weak Pull-Up Resistor* and *SDM I/O Internal Weak Pull-Up Resistor* tables. • Removed note about default VOD and pre-emphasis setting from the *HSIO Differential I/O Standards Specifications* table. • Updated the Receiver input eye specifications $V_{RX-DIFF-PKPK}$ to "closed eye" in the *Receiver Electrical Specifications* table.
2025.08.11	• Updated the specifications for TCK clock frequency (F_{JCP}) and TCK clock period (t_{JCP}) in the *HPS JTAG Timing Requirements* table. • Added description to the *System PLL Reference Clock (Using HVIO) Specifications* table. • Added Insertion Loss specification to the *Receiver Electrical Specifications* table.

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Document Version	Changes
	• Added Input clock or external feedback clock input duty cycle ($t_{EINDUTY}$) parameter in the *I/O PLL Specifications* table. • Updated the maximum specifications for Input clock frequency source (-6S and -7S) in the *I/O PLL Specifications* table. • Updated the bit stream sizes for the variants in the *Configuration Bit Stream Sizes* table. • Revised the *HPS and SDM DC Characteristics* and *HPS and SDM I/O Standard Specifications*, organizing them into individual sections: — *HPS I/O DC Characteristics* — *SDM I/O DC Characteristics* — *HPS I/O Standard Specifications* — *SDM I/O Standard Specifications* • Updated the maximum specifications for Clock Frequency f_{HSCLK_in}(input clock frequency) SLVS400 I/O Standards in the *Agilex 3 FPGAs LVDS SERDES Specifications* table. • Updated the specifications in the *Programmable IOE Delay Specifications* table. • Updated the conditions of Tri-stated pin to V_O in the *HVIO Pin Leakage Current* table. • Added footnote about receiver compliance to the V_{OH} in the *MIPI D-PHY Low-Power I/O Standards Specifications* table. • Updated the HDMI 2.1 Lane rate specifications in the *Electrical Compliance List* table. • Updated the fixed point multiplication modes specifications in the *Agilex 3 FPGAs DSP Block Performance Specifications for Single DSP Block* and *Agilex 3 FPGAs DSP Block Performance Specifications for Multiple DSP Blocks* tables • Updated the MLAB and M20K block memory specifications (-6S and -7S) in the *Agilex 3 FPGAs Memory Block Performance Specifications* table.
2025.04.28	Initial release.